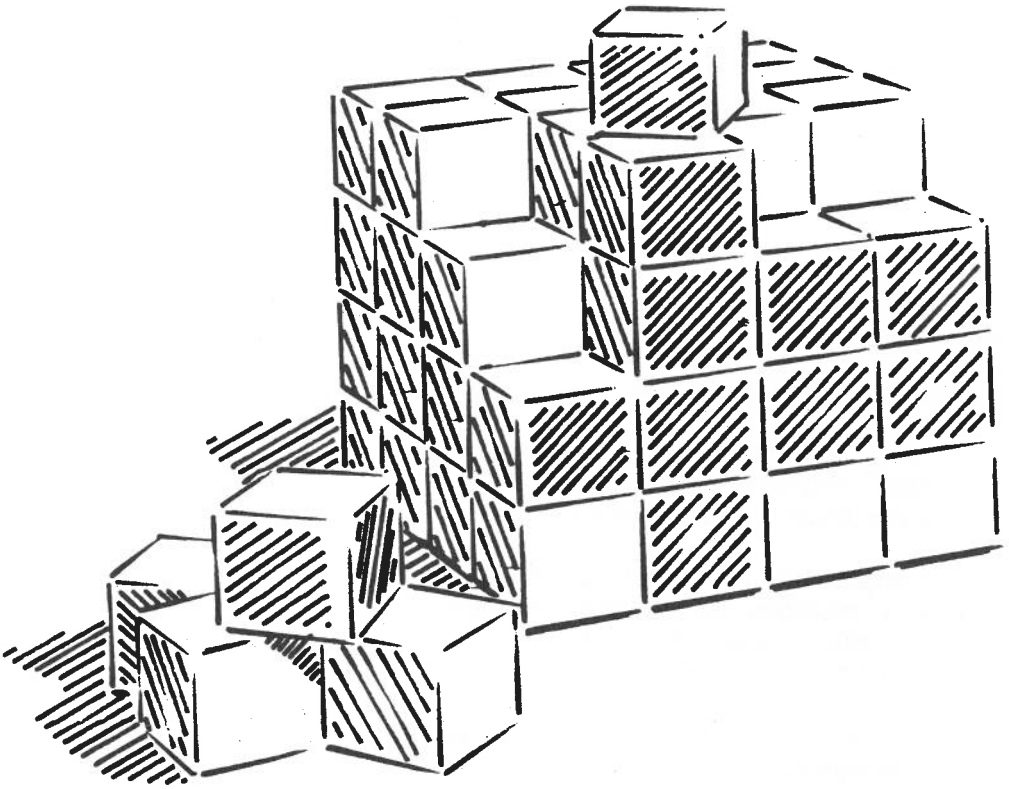
P3100 PC

Technical reference manual



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A publication of:

Philips Data Systems
SSS - Training & Documentation
Apeldoorn, The Netherlands

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Order Number 5122 993 82831

Manual Number F130H

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Section 1
SYSTEM OVERVIEW

INTRODUCTION

This PC Technical Reference Manual provides information to support the Desktop PC, the Portable PC, and the Hard Disk Drive. These products are designed to be compatible with IBM Personal Computer hardware, firmware, and software.

This manual is designed to provide information for the producers of application programs, firmware, and hardware as well as for end users, specifically:

- Designers and programmers of PC software.
- Programmers and technicians responsible for special applications.
- Manufacturers of PC expansion boards and peripherals.
- Users of Desktop and Portable PCs and Hard Disk Drives who require design information beyond the scope of the PC User's Guide, and the PC Service Manuals.

The PC Technical Reference Manual is organized into five sections with appendices, as follows:

Section 1: System Overview
Technical design and operating features of the Desktop PC, Portable PC, and Hard Disk Drive.

Section 2: Logical Operations
Main PCB logic, CPU, memory, timers, buses, controllers, signals, and I/O functions.

Section 3: Inputs and Outputs
Ports, registers, buffers, and signals for I/O channel and I/O interfaces.

Section 4: Super-Resolution Graphics
Characters, graphics, memory locations, and assembly language programming.

Section 5: ROM BIOS
Access to BIOS through vectors, interrupts, command codes, and registers.

Appendices A-F: PC publications and references, circuit diagrams, glossary, BIOS listing, keyboard functions, and system memory map.

HARDWARE DESCRIPTION

The PC is an advanced personal microcomputer that provides a large user memory capacity and a high level of hardware flexibility. It uses a 16-bit microprocessor, which allows for high-speed operation and powerful graphics and data handling capabilities.

The PC consists of the three major units: the system unit, the keyboard, and the monitor.

The system unit contains an 8088 central processing unit, memory, control circuits, interface logic, and high-resolution graphics. The main PC board supports 128K to 512K of memory. The input/output interfaces integral to the system unit include: serial port, parallel port, floppy disk drives (two), and a super-resolution monitor. There are four expansion slots that can be used to connect peripheral devices, such as an optional color monitor, and an optional internal or external hard disk drive.

The keyboard has 83 keys, including typewriter keys, 10 special function keys, a numeric keypad, and special keys required for computer operation. The keyboard has a separate microprocessor that strobes the keyboard and sends coded information to the system unit.

The monitor has a nonglare screen and excellent resolution. Its high-resolution characters and graphics with a green or amber phosphor insure a level of eye comfort unusual for desktop computers.

The 10-Megabyte hard disk drive can be installed in place of the second disk drive in the Desktop PC, or used externally with the Portable PC. The hard disk provides storage that exceeds the capacity of 30 double-sided floppy disks. It can read and write at greater speed than the floppy disk drive.

The Desktop PC and Portable PC come equipped with at least 128K of RAM, and one 5¼-inch, double-sided, double-density floppy disk drive. The maximum storage capacity for a floppy disk is 320K in 8-sector format (DOS 1.25) and 360K in 9-sector format (DOS 2.0). The main PC RAM can be increased in steps of 128K to a maximum of 512K. Several combinations of disk drives can be installed in the system unit, up to a maximum of two floppy disk drives and one 10-Megabyte hard disk drive.

Table 1-1 shows the specifications for the Desktop PC (PC-1) and the Portable PC (PC-2).

Table 1-1
SPECIFICATIONS

ITEM	DESCRIPTION
MODEL PC-1	
Memory	128K (expandable to 512K)
Storage type	Double-sided, double-density floppy
Number of drives	1 (expandable to 2)
Disk capacity	320K with DOS 1.25 (8-sector); or 360K with DOS 2 (9-sector)
RAM-disk	Yes

Table 1-1
SPECIFICATIONS (Continued)

ITEM	DESCRIPTION
Monitor type	High-resolution green or amber phosphor; nonglare, wide-view screen
Monitor screen size	Desktop: 12-inch diagonal Portable: 9-inch diagonal
Keyboard	Detachable, IBM PC configuration, 83 low-fatigue capacitance keys
Keyboard indicators	Number and caps lock
Keyboard cable	6-ft coil connects to front of system
Processor	16-bit 8088
Communications port	1 RS-232C serial
Printer port	1 Centronics-compatible parallel
Video port	Desktop only
Expansion slots	4 IBM PC-compatible slots
Power supply	110-watt switching supply
Alphanumeric display	80 columns, 25 rows
Character font	16 x 13 dots
Character attributes	Reverse video, underline, blinking, high intensity
Graphics resolution	640 x 325 pixels
Text with graphics	Text can overlay graphics
Graphic storage	Up to 8 graphic pages with 256K
Dimensions	Desktop PC system unit-19.5 x 16.8 x 6.3 inches Portable PC (monitor included)-20 x 16 x 9 inches
Weight	Desktop PC system unit* - 28.3 pounds Desktop PC monitor - 19.2 pounds System unit plus monitor - 47.5 pounds Portable PC - 38.6 pounds

* Includes weight of keyboard and cables.

Table 1-1
SPECIFICATIONS (Continued)

ITEM	DESCRIPTION
MODEL PC-2	
	Same as Model PC-1, with:
Number of drives	Two
MODEL PC-HD (Desktop only):	
	Same as Model PC-1, with:
Storage type	Double-sided, double-density floppy
	Winchester hard disk
Storage capacity	Floppy disk, 320K or 360K
	Hard disk, 10 Megabytes
OPTIONAL HARDWARE:	
Memory	Up to 512K in 128K increments
Disk	Second floppy disk drive
	External Winchester hard disk (10 Megabytes)
SOFTWARE PROVIDED (all PCs):	
Operating system	DOS 1.25 (8-sector)
Language	GWBASIC
Applications	MultiMate (word processor) PC TUTOR (self-teacher)
TECHNICAL PUBLICATIONS:	
Recommended PC technical publications are listed in Appendix A.	

SYSTEM UNIT

The system unit consists of the case; the inner assembly, which includes front and back panels, power supply, and disk drive(s); and the main PC Board (PCB), which includes the CPU, memory, logic, interfaces, and expansion slots. Figure 1-1 shows the case, inner assembly, and PCB.

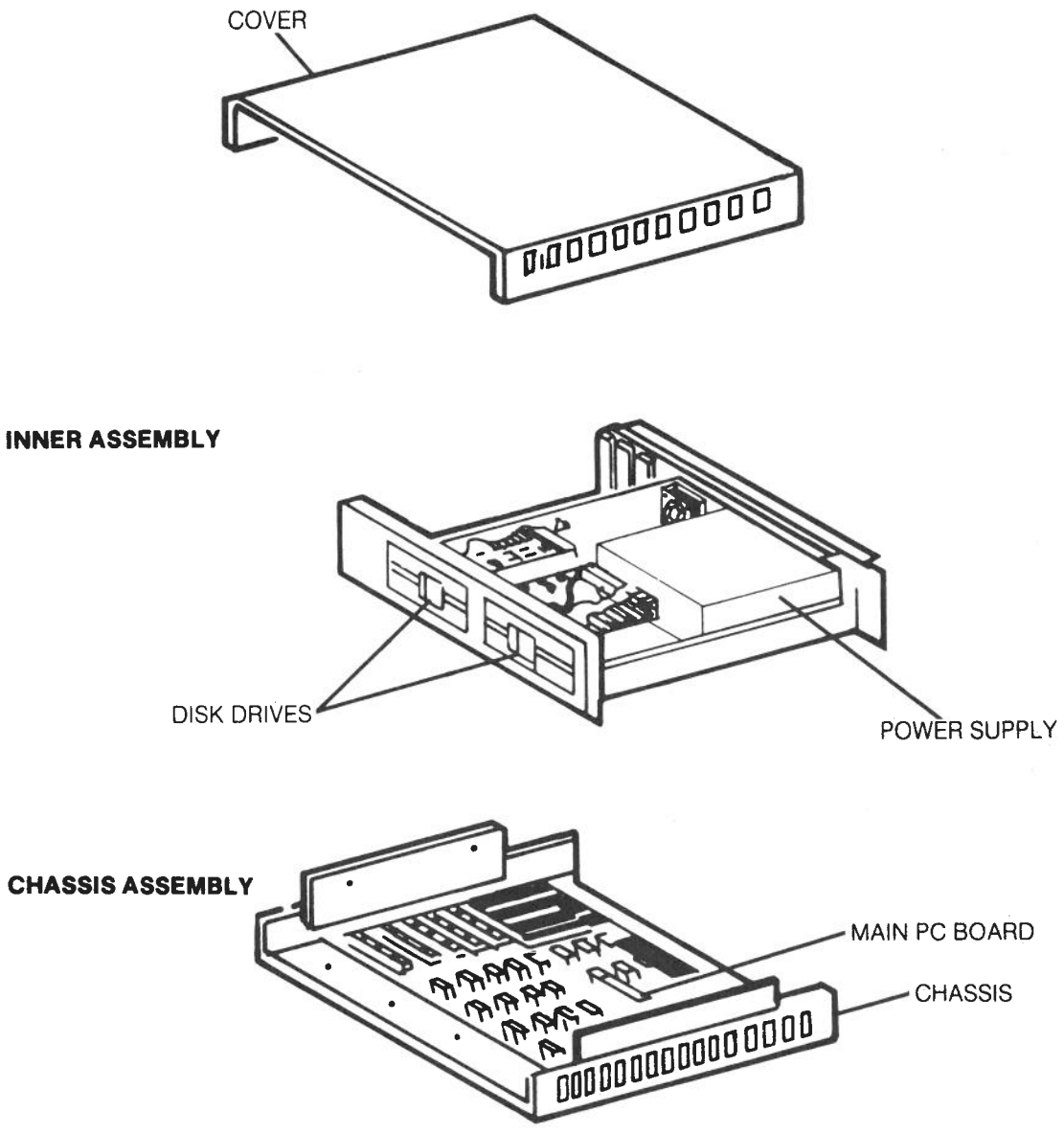


Fig. 1-1. PC system unit showing inner assembly and PCB

Disk Drives

The disk drives provide bulk storage for any programs or data the operator may wish to use. On the appropriate command from the microprocessor, the drive unit reads data from, or writes data to the disk. This may be either a 5¼-inch floppy disk or a hard disk, depending on the I/O options selected by the user.

The Main PC Board

Figure 1-2 shows the layout of the principal components on the main PC board (PCB) for the Desktop PC. Figure 1-3 shows the PCB for the Portable PC. Expansion boards are mounted above the memory on the left side of the chassiss. Serial, parallel, and video connectors are at the rear, the keyboard connector at the front, floppy disk connector at the center, and light pen connector internal at the rear. These figures show the locations of switches, jumpers, and connectors for the Desktop PC and Portable PC.

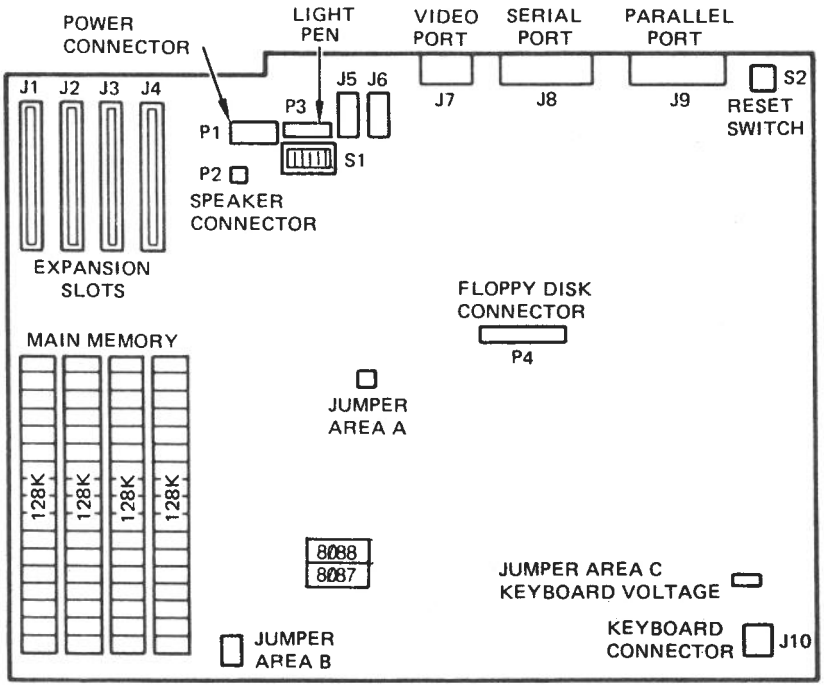


Fig. 1-2. Desktop main PC board

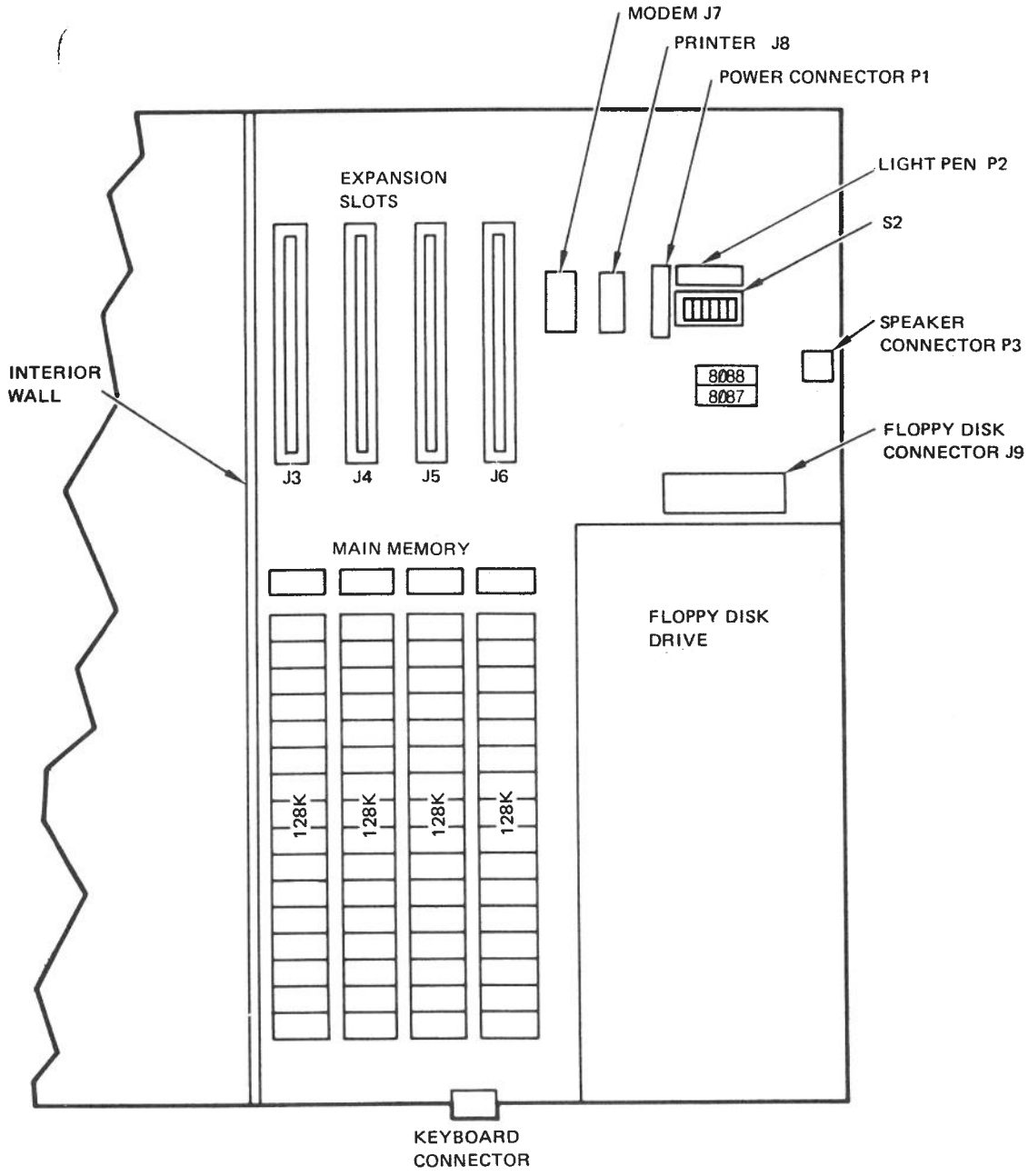
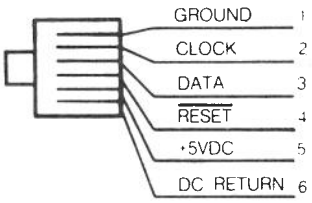


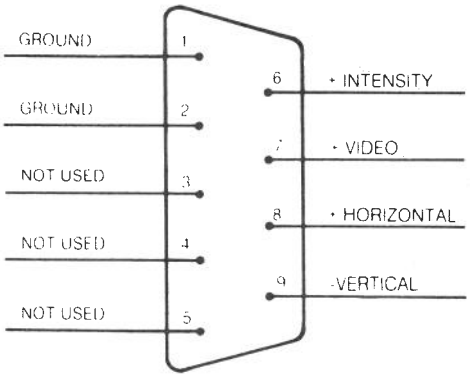
Fig. 1-3. Portable main PC board

Figure 1-4 shows the pin designation for all external connectors.

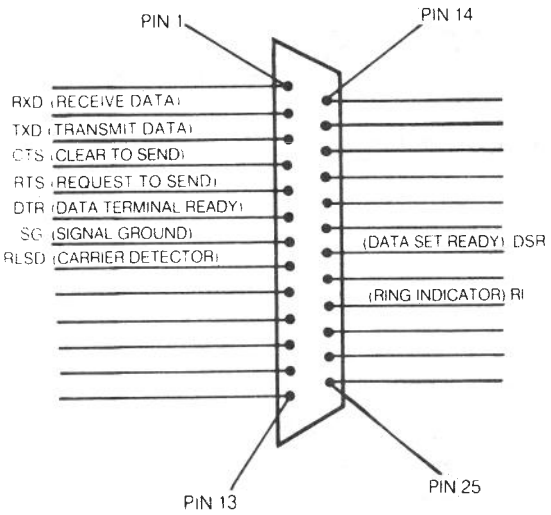
Table 1-2 shows the switch and jumper settings to configure the system and system interfaces for both the Desktop PC and Portable PC.



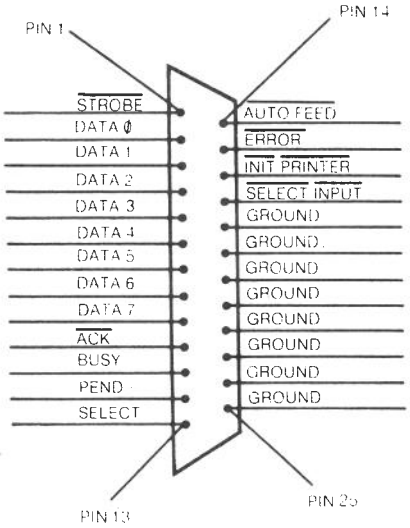
KEYBOARD CONNECTOR



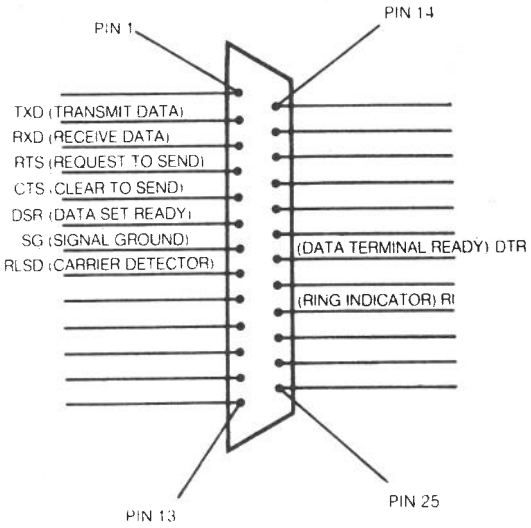
MONITOR CONNECTOR
(Desktop PC Only)



SERIAL OUTPUT CONNECTOR (DCE)



J9-PARALLEL OUTPUT CONNECTOR



SERIAL OUTPUT CONNECTOR (DTE)

Fig. 1-4. External connectors on system unit

Table 1-2
SWITCH AND JUMPER SETTINGS
SWITCH S1 (Desktop) or S2 (Portable)

SWITCH	CONFIGURATION	SWITCH SETTING
1	8087 not installed	on
	8087 installed	off
2	1 floppy disk in system	on
	2 floppy disk in system	off
3 & 4		3 4
	Signal-to-video connector disconnected	on on
	Low-resolution color graphics	off on
	High-resolution color graphics	on off
	Monochrome	off off
5 & 6		5 6
	128K of memory installed	on on
	256K of memory installed	off on
	384K of memory installed	off off
	512K of memory installed	off off

Internal Settings

Jumper Area A

(Set at factory)
IN for U105 (Desktop) or U87 (Portable) is a 2764 (8K PROM)
OUT For U105 (Desktop) or U87 (Portable) is a 27128 (16K PROM)

Jumper Area B

(Desktop unit only)
1 to 3 — Graphics set in second 256K
2 to 4 — Graphics set in first 256K

Jumper Area C

(Set at factory)
1 to 2 — +12VDC to keyboard
2 to 3 — +5 VDC to keyboard

Serial Interface Option

To use the serial port as a modem interface (DCE): insert platform in jumper J6 (desktop) or J7 (portable)

To use the serial port as a serial printer interface (DTE): insert platform in jumper J5 (desktop) or J8 (portable)

POWER SUPPLY

The power supply is voltage regulated and surge-protected. It is designed for a maximum continuous load of 110 watts, and accommodates voltage variations from 95 to 150 volts (110 volt) or 180 to 234 volts (230 volt) and frequencies ranging from 47 to 63 Hz. The 5 vdc supply is regulated within 1%, and the 12-volt supply within 3%. Table 1-3 gives the power supply specifications.

Table 1-3
POWER SUPPLY SPECIFICATIONS

INPUTS:	95-150 volts AC (110 volt) 180-234 volts AC (230 volt)	47-63 Hz 47-63 Hz
OUTPUTS:	5 vdc at 9.5 amps (over-voltage protected at 6.2 vdc ± 0.4 vdc) 12 vdc at 3.0 amps (6 amps peak) 12 vdc at 1.5 amps (3-terminal regulator) -12 vdc at 0.25 amps	
LOAD REGULATION:	5 vdc ±1% all others ± 3%	
RIPPLE:	5 vdc 50 mv peak-to-peak all others 100 mv peak-to-peak	
HOLD-UP TIME:	16 microseconds minimum	

The main board with 512K of memory requires 4 amps at 5 vdc. This enables a rated output for expansion slots of 4 amps at 5 vdc. The 12-vdc power supplies are sufficient for the expansion slots, the two floppy disks, and one hard disk drive. Additional drives will require an external power supply. The super-resolution monitor (or color monitor) is powered externally. The monitor is integral to the Portable PC unit and accesses the external power source.

Expansion Slots

The computer has four expansion slots located in the left rear area of the main PCB. These are board-edge connectors into which optional controller PCBs can be inserted. The expansion slots make power and microcontroller signals available to any optional PC boards the user may wish to install. Expansion slots enable peripherals (such as a color monitor or a rigid disk drive) to be connected to the basic system.

Section 2
LOGICAL OPERATIONS

MAIN PC BOARD OVERVIEW

Figure 2-1 shows the major functions of the Main PC Board. Circuit and block diagrams for the Desktop and Portable PC are presented in Appendix B. Signal names are defined in Appendix C.

The 8088 Central Processing Unit (CPU) is the heart of the system. Figure 2-1 shows the relationship of the CPU to the buffers, controllers, memory, clock generator, BIOS ROM, I/O interfaces, and peripheral devices.

An 8087 numeric co-processor, when installed, increases the speed of arithmetic computations. It is connected in parallel with the 8088.

The system clock generator is connected to the CPU to control system timing. An interrupt controller communicates interrupt requests from the keyboard, floppy disk drives, I/O ports, and expansion slots.

CPU data and address lines are connected to buffers, and the control lines are connected to a bus arbitrator and controller. The bus controller decodes and demultiplexes the data/address signals for the system data, address, and control buses.

The Input/Output (I/O) ports, floppy disk controller, system memory, video control logic and screen memory all communicate with the CPU through the system buses.

The system memory capacity is 128K minimum to 512K maximum. Memory may be expanded in 128K increments.

The Basic Input/Output System (BIOS) Read Only Memory (ROM) is connected to the CPU through the system buses. When the system goes into power-up, the CPU addresses the BIOS ROM and receives instructions for booting the system. System and keyboard routines, parameters, and variables are provided by the BIOS ROM.

The video control logic and screen memory provide the video signals to the monitor. The video control logic also can access the system memory where high-resolution graphics are stored.

The I/O ports read inputs from the keyboard and configuration switches, and serve as inputs and outputs to the serial and parallel ports and expansion slots. The floppy disk controller supplies the signals necessary to control the disk drives.

The Direct Memory Access Controller (DMAC) manages the transfer of data between memory and peripheral devices, such as a floppy disk, without going through the CPU. This enables rapid transfer of large blocks of data. The DMA Controller is connected to the bus arbitrator, which switches control of the system buses from the CPU to the DMAC during the direct memory access operation.

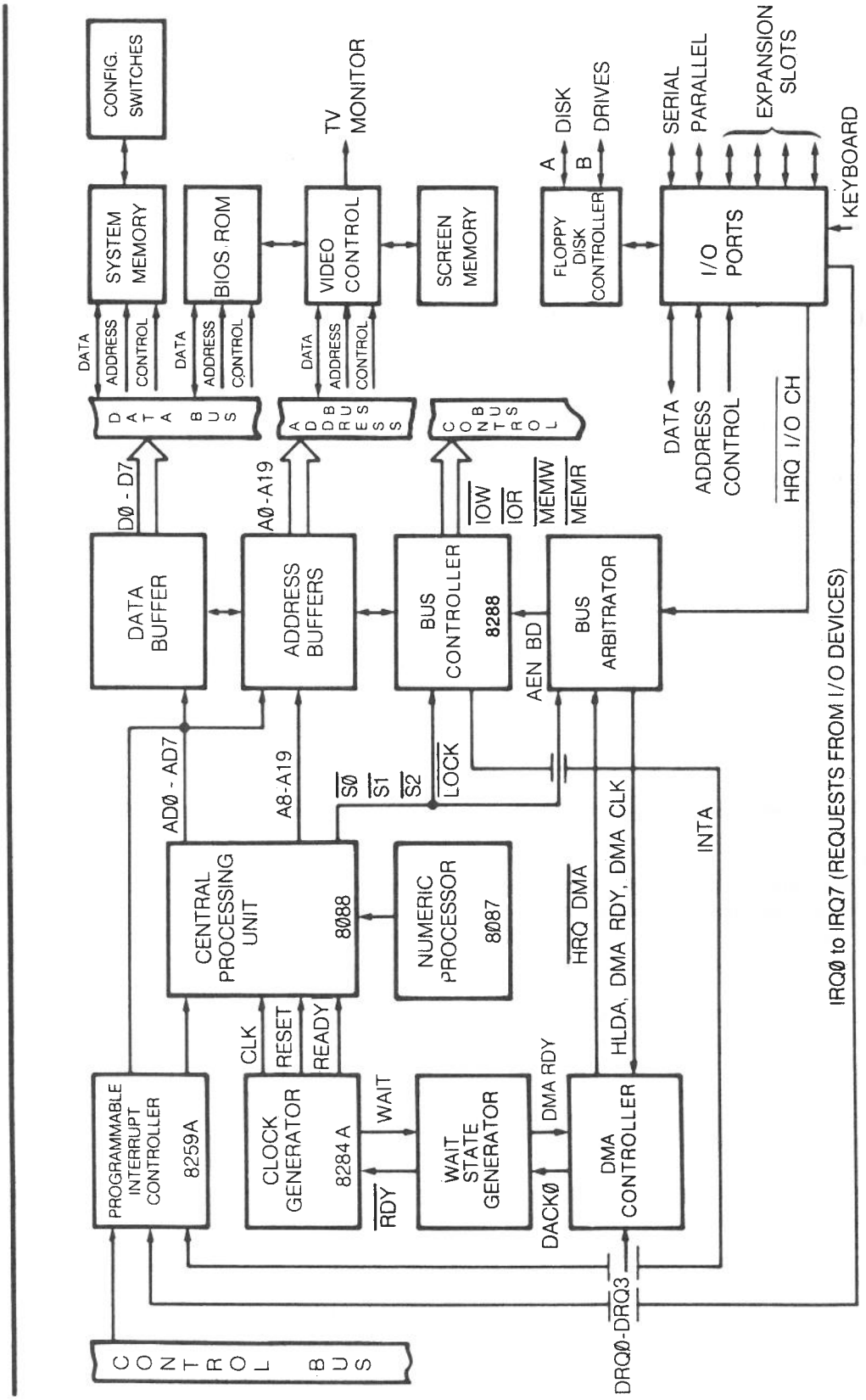


Fig 2-1. Principal functions of the main PC board

CENTRAL PROCESSING UNIT (CPU)

The Intel 8088 microprocessor has 16-bit internal architecture with an 8-bit data bus. Twenty address lines make it possible to address one megabyte of memory directly. The 8088 CPU can achieve 16-bit hardware speeds with the economy inherent in 8-bit systems.

In this computer, the 8088 operates in the maximum mode. The CPU shares its control functions with an external bus controller (8288) and an optional numeric co-processor (8087). This configuration provides the flexibility needed for implementing large system features such as high-resolution graphics and fast computation.

Communication with the bus controller and bus arbitration logic is accomplished by means of the CPU status signals $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, and $\overline{LOCK}$. The lock signal prevents control of the system buses from being transferred from one bus master to another at the incorrect time.

$\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ provide coded information that is used by the bus controller to generate the control signals. This coded information also is used by the bus controller to monitor the CPU status.

The bus controller generates the INTerrupt Acknowledge signal, INTA, that goes to the interrupt controller when an interrupt request is made.

NUMERIC CO-PROCESSOR

The 8087 numeric processor is used to increase the speed and precision of arithmetic operations. It is connected in parallel with the 8088 with four control lines for communication with the CPU. The 8087 responds to instructions that are not in the 8088 instruction set. When one of these instructions occurs, the 8088 does not respond, while the 8087 recognizes the instruction and executes it.

If an error is detected (for example, the 8087 is instructed to perform an impossible calculation), the NP INT signal is generated by the 8087. The NP INT signal generates a NonMaskable Interrupt (NMI) signal that is sent to the 8088 CPU. This signal causes the CPU to vector to an appropriate subroutine for handling the error. Either the interrupt is cleared by the CPU, or the system is reset.

CLOCK GENERATOR

The clock frequency generator is used for timing system functions, including peripheral hardware, using ReaDY (RDY) and WAIT signals. Figure 2-2 shows the input and output signals from the 8284A clock generator.

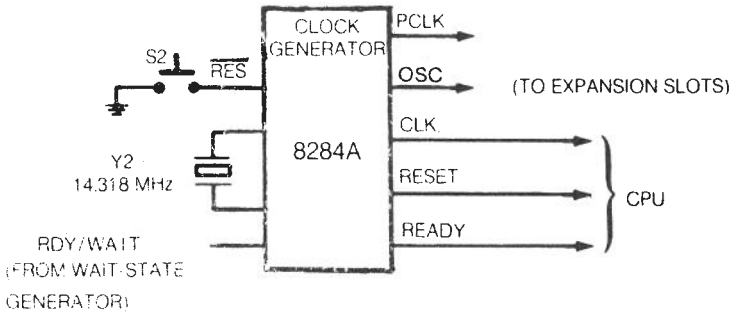


Fig. 2-2. Clock generator input and output signals

Timing for the CPU comes from the 8284A clock generator, which produces the clock frequency (CLK) needed for proper operation of the 8088 and 8087 processor and co-processor. The crystal oscillator produces a frequency of 14.31818 MHz, which is divided by three to produce the 4.77 MHz CLK frequency for the 8088 processor. The crystal frequency is divided by four to produce the 3.58 MHz colorburst frequency for color video monitors. The PCLK output, which is half the frequency of the CLK signal, is used by the Programmable Interval Timer for timing peripheral devices.

The clock generator produces the RESET signals used to stop and restart the processor and to initialize the system logic. The system can be reset manually using the switch on the back of the system unit. RESET stops all current processing activity and reboots the system.

The ReaDY ($\overline{RDY}$) signal from the clock generator is used to synchronize the CPU with slower I/O devices, memory, and peripherals. When necessary, it places the CPU in a waiting state in response to the $\overline{RDY}$/WAIT signal from the wait-state generator.

The address and data buses from the CPU are connected through buffers to the main system buses. The eight lowest bits of the address bus are multiplexed with the data bus. Data and addresses are demultiplexed by the bus controller.

BUS ARBITRATOR, BUS CONTROLLER, WAIT-STATE GENERATOR

The bus arbitrator and the bus controller work together to assign control of the system buses to the 8088/8087 processor or to the 8237A DMA controller. Figure 2-3 shows the specific control signals and functions involved.

The 8288 bus controller decodes the $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ status lines from the CPU and generates the control bus signals. It also generates the Address Latch Enable (ALE), Data ENable (DEN), and Data Transmit/ Receive (DT/$\overline{R}$) signals that are used to demultiplex the CPU's buses. The Address ENable BD (AEN BD) signal from the bus arbitrator enables these signals, while ALE latches their addresses onto the system bus.

The DEN signal enables the data buffer to transfer data between the CPU and the system data bus. The DT/$\overline{R}$ signal determines the direction of these transfers. Bus control timing is shown in Fig. 2-4.

The function of the wait-state generator is to signal the clock generator (via the $\overline{RDY}$/WAIT signal) that the 8237A DMA Controller (DMAC) is taking over. It holds the processor in a waiting state until the DMA transfer is completed. Another function of the wait-state generator is to produce a DMA ReaDY (DMA RDY) signal to the DMAC, which prepares the DMAC to interface with slow memories and peripheral devices.

PROGRAMMABLE INTERRUPT CONTROLLER

The 8259A Programmable Interrupt Controller prioritizes and services interrupt request signals from I/O interfaces and devices. Figure 2-5 shows input signals to and output signals from the interrupt controller.

In addition to the 8087 and the 8237A DMAC, there are several other components that must occasionally interrupt processor execution. These include the floppy disk controller, and devices connected to the I/O ports and expansion slots. Interrupt ReQuest (IRQ) signals from these sources go to the 8259A Programmable Interrupt Controller, which in turn sends an INT signal to the CPU.

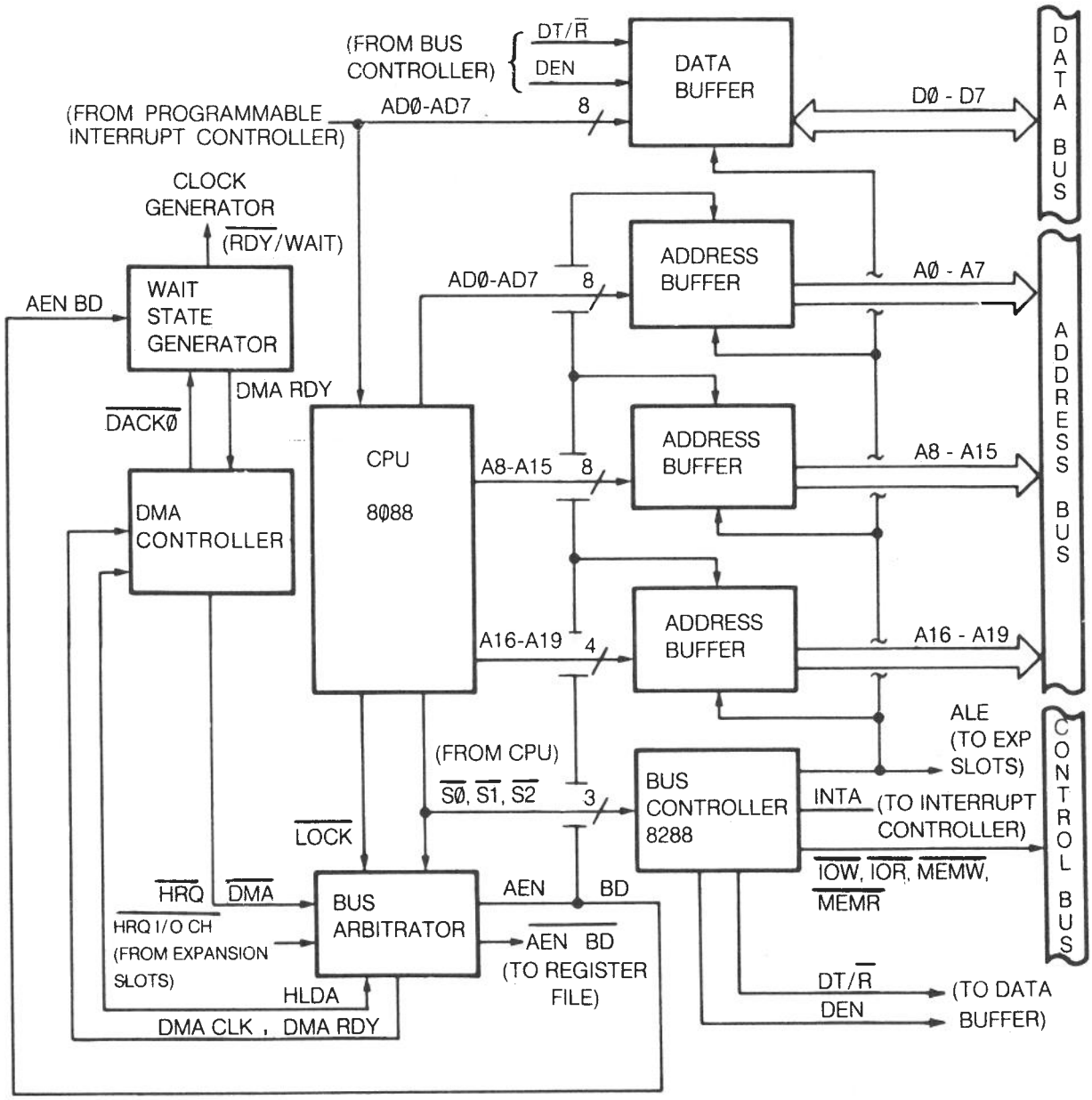


Fig. 2-3. Control signals for bus arbitrator, bus controller, and wait-state generator

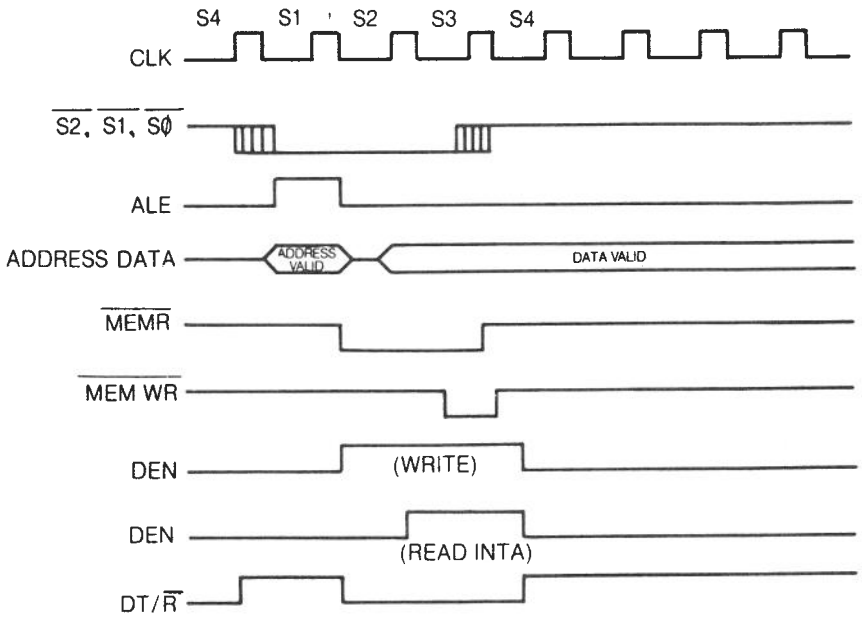


Fig. 2-4. Bus control signals and timing

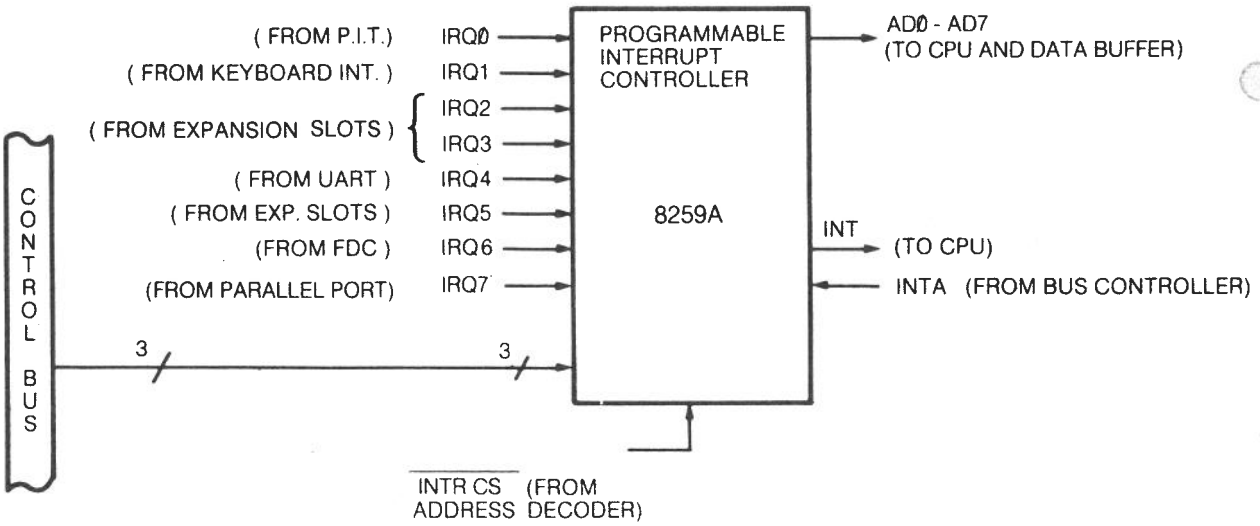


Fig. 2-5. Programmable interrupt controller input and output signals

The order in which interrupt requests are serviced is determined by priorities programmed into the interrupt controller. If two IRQ signals are received at the same time, the one with the lower number will be satisfied first.

When the processor is interrupted, an INTerrupt Acknowledge (INTA) is sent back to the interrupt controller by the bus controller, which receives status information from the CPU. The INTA causes the 8259A to output an interrupt vector address onto the data bus. This address tells the CPU where to go to fetch the interrupt subroutine for the device that is to be serviced.

DMA CONTROLLER

Data can be transferred between system memory and requesting devices without going through the CPU. The 8237A Direct Memory Access Controller (DMAC) takes over the system buses and operates in a single transfer mode. It is used to transfer data between floppy disk and memory, and to service other devices through expansion slots. Figure 2-6 shows the DMA controller input and output signals.

DMA control is accomplished when a DMA ReQuest signal (DRQØ-DRQ3) is sent to the DMAC from the requesting device. The DMAC sends a Hold ReQuest signal (HRQ DMA) to the bus arbitrator. The bus arbitrator, upon receiving the HRQ DMA signal, sends a HoLD Acknowledge signal (HLDA) to the DMAC and isolates the CPU from the data, address, and control buses. Upon receiving the HLDA signal, the DMAC sends a DMA ACKnowledge signal ($\overline{\text{DACK}}$Ø-$\overline{\text{DACK}}$3) to the requesting device and takes control of the system buses.

The control bus and the eight lower bits of the address bus (AØ-A7) are taken over by the 8237A DMAC through buffers. The Data lines on the DMAC (DØ-D7) are multiplexed with the higher order Address bits A8-A15. The DMAC takes control of A8-A15 of the address bus, which is latched by the ADdress STroBe (ADSTB) signal from the DMAC. The highest order address bits (A16-A19) are addressed through a register file. These addresses are stored initially under program control. Under DMA control they are used to address the DMA page numbers. Page numbers are stored in one of four registers selected by address lines AØ and A1. The page number or register that is output to the address bus is selected by either the $\overline{\text{DACK2}}$ or $\overline{\text{DACK3}}$ signals from the 8237A DMAC. Once the page number is selected, it is output by the AEN BD signal from the bus arbitrator. The timing diagram for the DMA control is shown in Fig. 2-7.

When the 8237A DMA Controller takes over the system buses, data can be transferred directly between the memory and the requesting device without going through the CPU. The DMAC is operated in the single transfer mode. When the transfer is completed, a Terminal Count (TC) signal is sent to the serviced device.

The DMA Controller is initially programmed by the CPU through a buffer. It is selected by an address decoder, which also selects the interrupt controller, the Programmable Interval Timer, and the Programmable Peripheral Interface.

PROGRAMMABLE PERIPHERAL INTERFACE

The main purpose of the 8255-5 Programmable Peripheral Interface (PPI) is to read information from the system configuration switches and the keyboard interface and transmit it to the CPU. The PPI is also used to turn on the speaker drivers.

Figure 2-8 shows the various inputs and outputs to the PPI, and the relationship of the PPI to the Programmable Interval Timer.

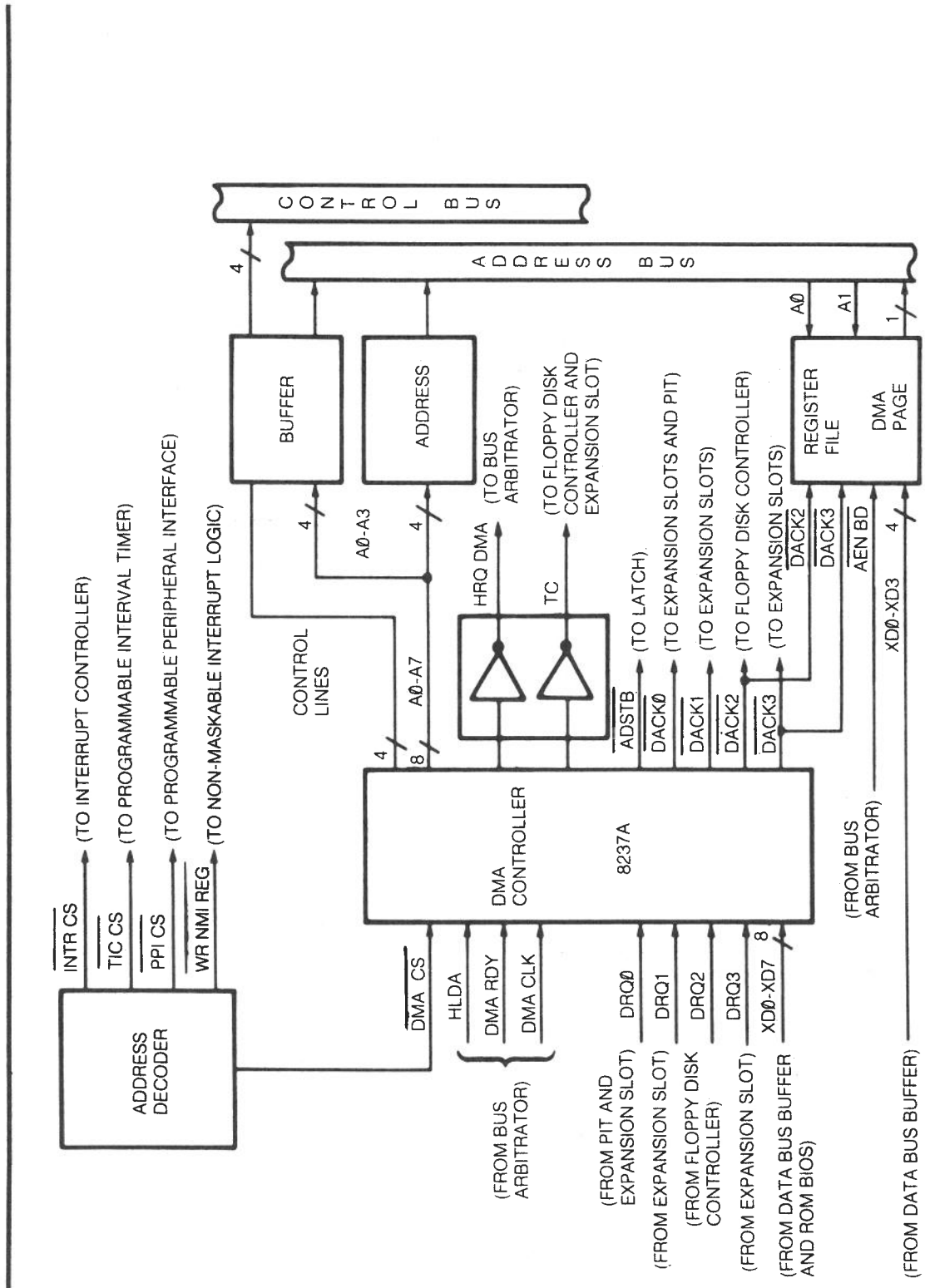


Fig. 2-6. DMA controller input and output signals

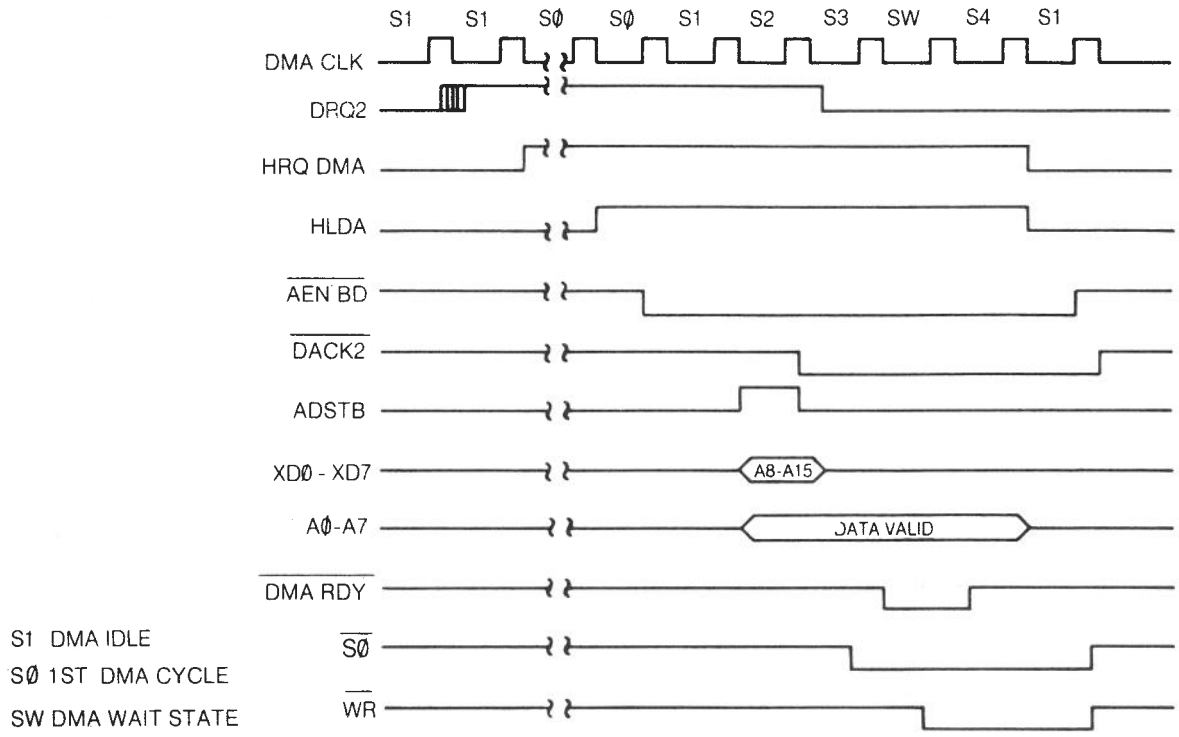


Fig. 2-7. DMA transfer signals and timing

The ports of the 8255-5 Programmable Peripheral Interface are initially set under program control. The 8255-5 PPI port A bits are programmed as inputs, while port B bits are programmed as outputs. Some of port C's bits are programmed as inputs and some as outputs. Data is transferred between the PPI and the data bus through a buffer.

The keyboard interface accepts the scan codes and serial data from the keyboard. It converts the serial data to parallel data and sends it to port A of the PPI. When the keyboard interface buffer is full, it sends a signal to a flip-flop, which sends an Interrupt ReQuest signal (IRQ1) to the CPU through the interrupt controller. The CPU then reads the contents of port A.

Positions 1, 2, 3, and 4 of the configuration switch block (S1 for the Desktop PC or S2 for the Portable PC) are latched and sent to port A of the PPI. The CPU reads this port immediately after power-up or reset to determine the configuration. It does not read this port again until a keyboard interrupt is sensed. Switches 5 and 6 on the configuration switch (S1 for the Desktop PC, S2 for the Portable PC) are connected directly to the input bits of port C. The CPU reads these bits immediately after power-up or upon reset.

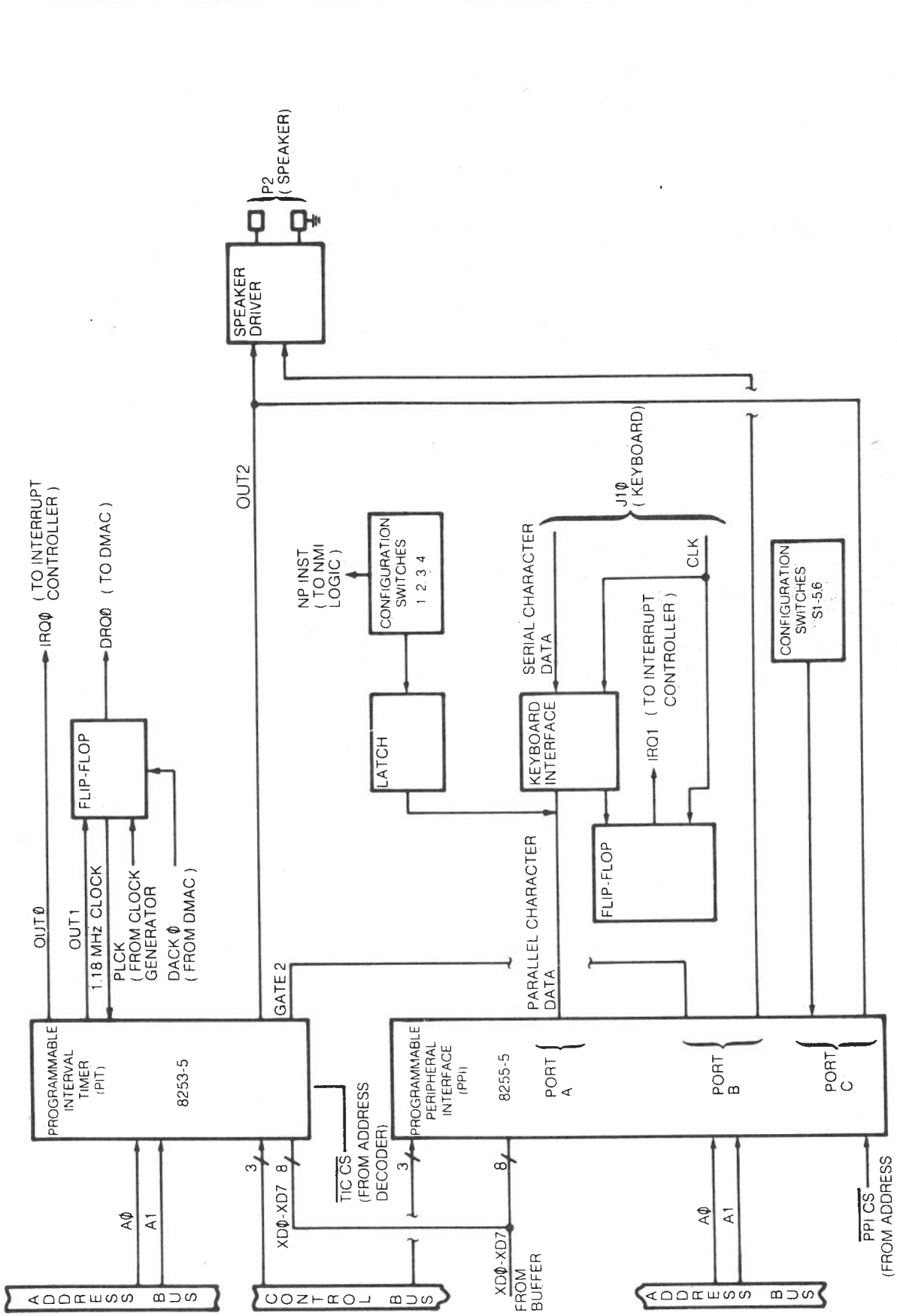


Fig. 2-8. Programmable peripheral interface and interval timer

PROGRAMMABLE INTERVAL TIMER

The 8253-5 Programmable Interval Timer (PIT) has three clock OUTputs (OUTØ, OUT1, and OUT2). OUTØ generates Interrupt ReQuest IRQØ, which causes the interrupt routine that updates the time-of-day clock. OUT1 generates the Data ReQuest signal DRQØ, which is used to generate memory refresh for memory devices attached to expansion slots. OUT2 is used as the tone frequency for the speaker.

The Programmable Interval Timer is initialized under program control. It has internal registers that are addressed by AØ and A1, and it is programmed through the XD data bus. The Programmable Interval Timer is selected by the Time Interval Controller Chip Select (TIC CS) signal from the address decoder.

BIOS ROM

The Basic Input-Output System Read-Only-Memory (BIOS ROM) contains the instructions to load the operating system from disk drive A. It also contains the keyboard routines and I/O control programs. It is addressed by Address lines AØ-A13, and its instructions are communicated to the CPU via a buffer.

Section 5 describes key functions of the BIOS ROM in greater detail, and Appendix D lists code, data locations, interrupts, and other information on the ROM.

VIDEO CONTROLLER

The 6845 video controller provides the control signals to drive the video monitor. It has six basic functions:

- Refresh addressing to the screen and system memory.
- Row selecting to the character generator (LØ-L3).
- Timing signals for the video monitor (HSYNC, VSYNC).
- Cursor output.
- Display enable output.
- Light pen input.

The video controller refresh address lines and the system bus address lines are connected to multiplexers, whose outputs are connected to the address lines of the screen memory RAM and character attribute RAM. This enables both the CPU and the video controller to have access to these RAMs. The 2M signal from the video timing logic determines when each one can access the RAMs. Figure 2-9 shows the logic associated with video processing, timing, and control.

When the 6845 video controller is accessing the screen memory and character attribute RAMs, the data output of the screen memory is latched. The latch output is sent to the character generator ROM address lines along with the row-select outputs from the video controller. The character line selected is output from the character generator to shift registers that convert the parallel input to a serial output and send it to the video process logic. The video process logic drives the video monitor.

The output of the character attribute memory, which is accessed at the same time as the screen memory, is latched. The output of the latch is sent to the video process logic where it is decoded and used for video enhancements such as highlighting, blinking, underlining, and reverse video.

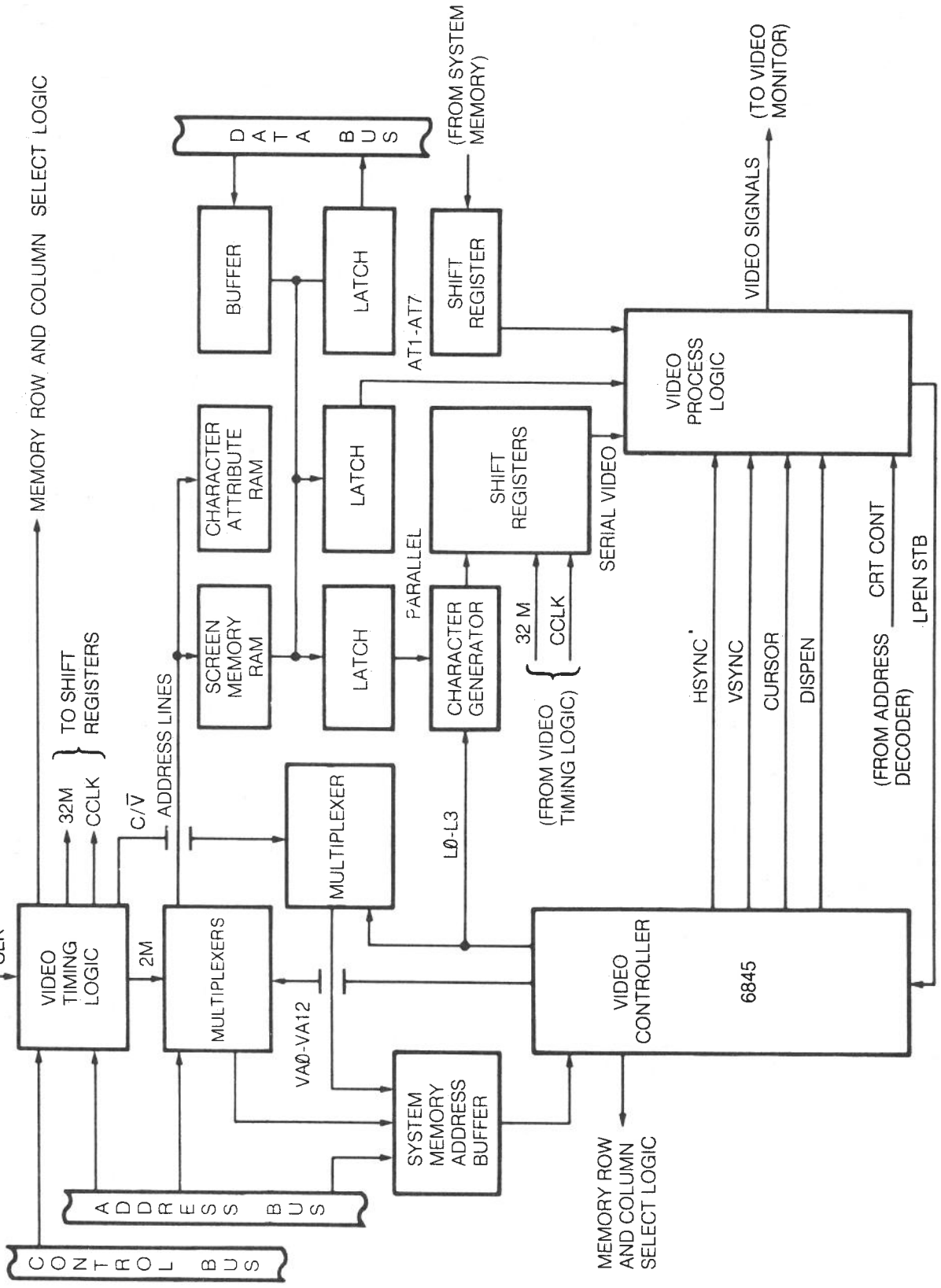


Fig. 2-9. Video logic and monitor interface

The CPU accesses the screen memory and character attribute RAMs either to update the screen memory and character attribute memory or to read their contents to the system data bus. Data is written into the RAMs from the data bus through buffers, and the RAMs' contents are read to the data bus through latches.

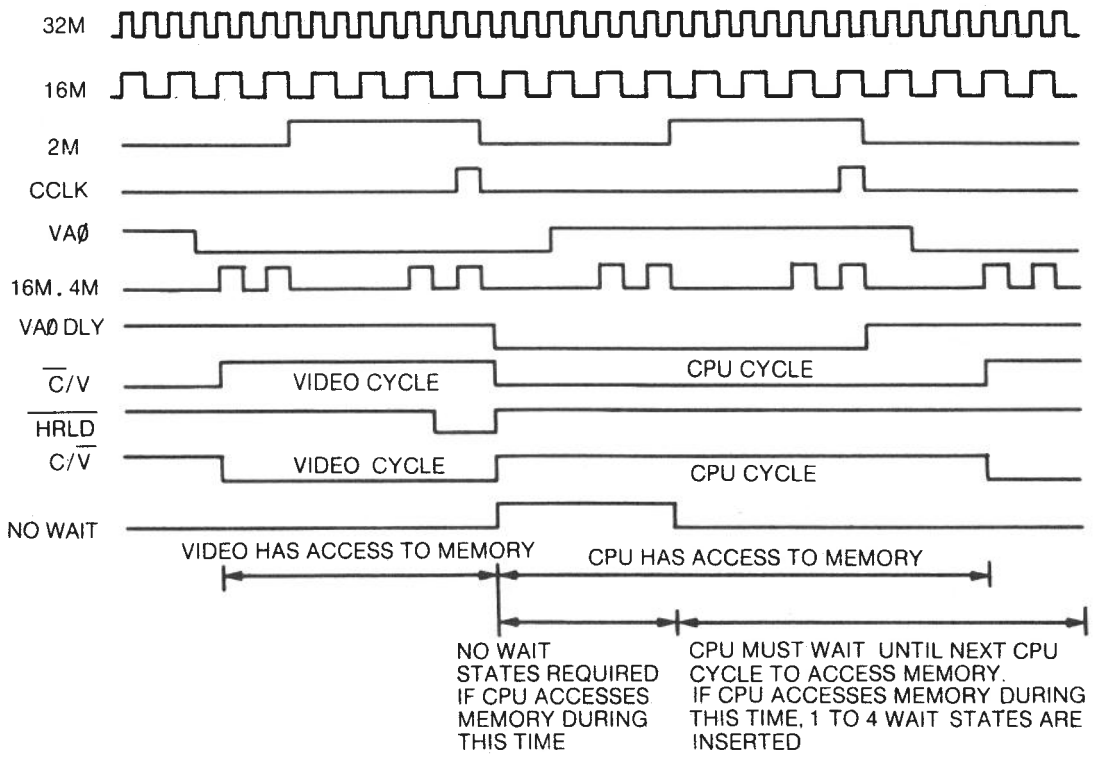
The video controller also accesses the system memory to perform a refresh or to access the high-resolution graphics. The refresh is accomplished through the Video controller Address lines (VAØ-VA12), and the row-select Lines (LØ-L3) are connected to multiplexers whose output is sent to the input of the system memory address buffer. When the multiplexer is enabled by the CPU Video timing logic signal ($C/\overline{V}$), the video controller accesses the system memory.

To display the high-resolution graphics, the output of the system memory is sent to shift registers where it is converted to a serial output and sent to the video process logic.

VIDEO TIMING, PROCESS, AND LIGHT PEN LOGIC

Inputs to the video timing logic include a 34.37 MHz crystal oscillator, the address bus, and the control bus. The timing logic processes all these inputs and produces the timing and control signals for the video controller, video process logic, and the memory row and column select logic.

The crystal oscillator is divided down and its outputs combined with other logic to produce the video timing signals. The video timing is shown in Fig. 2-10.



NOTE: IF CPU IS ACCESSING MEMORY WITH NO IDLE STATES BETWEEN MEMORY ACCESSES, THE AVERAGE NUMBER OF WAIT STATES IS LESS THAN ONE.

Fig. 2-10. Video signals and timing

The video process logic combines serial video signals, character attribute signals, the display enable signal, and the cursor signal to produce the video signal that drives the monitor. It also processes the horizontal and vertical sync signals to provide the proper timing signals to the monitor. The video sync timing is shown in Fig. 2-11.

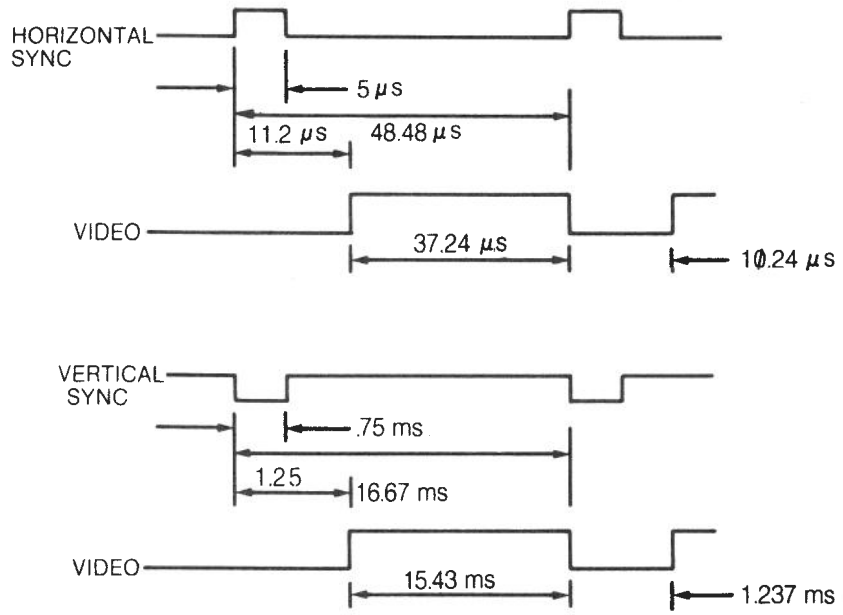


Fig. 2-11. Video sync signals and timing

The Light PEN STroBe signal (LPEN STB) is sent to the video controller, which uses this information to store the refresh address of the light pen input location. Figure 2-12 shows inputs and outputs to the light pen logic.

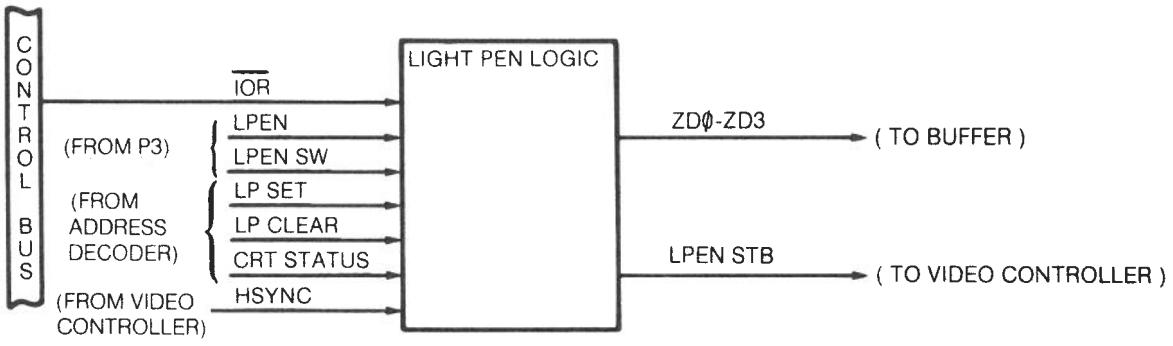


Fig. 2-12. Light pen logic

MEMORY ROW AND COLUMN SELECT LOGIC

The memory row and column select logic receives its inputs from the address bus and video timing logic. It processes these inputs to produce the Column Address Select signals (CASØ-CAS7) and the Row Address Select signals (RASØ-RAS1). These signals are used along with the address bus to select any cell in the system memory.

The memory row and the column select logic decodes the address bus, the Video controller Address bit VA13, and jumper "B" to produce the CAS signals. The logic divides down the 32M frequency from the crystal oscillator to produce the Row Address Select (RAS) signals. It also generates the Address MUltipleX (AMUX) signal that is used to multiplex the system memory address multiplexers.

The jumper "B" input determines which 256K block of memory will be used for graphics storage. Video controller Address bits VA11, VA12, and VA13 are used (with the jumper input) to select any 32K block within the graphics storage area (256K) as the display memory. This allows for rapid changes from one image to another on the screen. Figure 2-13 shows the relationship of the address bus to video timing logic and system memory.

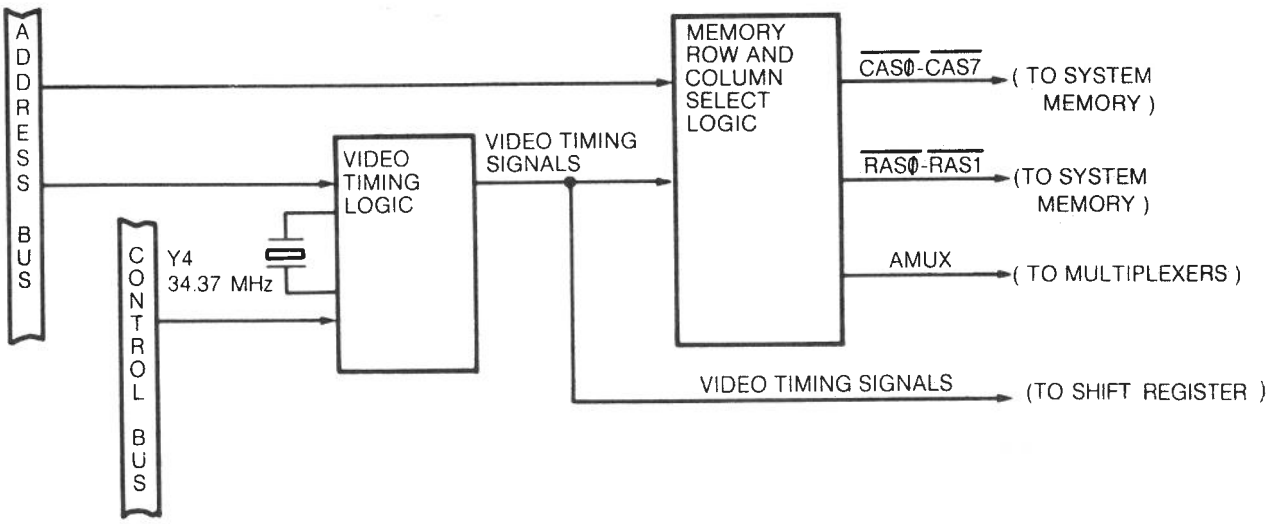


Fig. 2-13. Memory row and column select logic

SYSTEM MEMORY

The system memory is addressed by the CPU through multiplexers and through the Row Address Select ($\overline{RAS}$) and Column Address Select ($\overline{CAS}$) signals from the memory row and column address select logic. When memory write signals are supplied, data is written from the data bus through a buffer into memory. Memory contents are read to the data bus through buffers. Figure 2-14 shows the various inputs to and outputs from system memory.

Address bus multiplexers are enabled by the video timing logic so that the video controller and the CPU do not access the system memory at the same time. The system memory is refreshed by the video controller through address multiplexers.

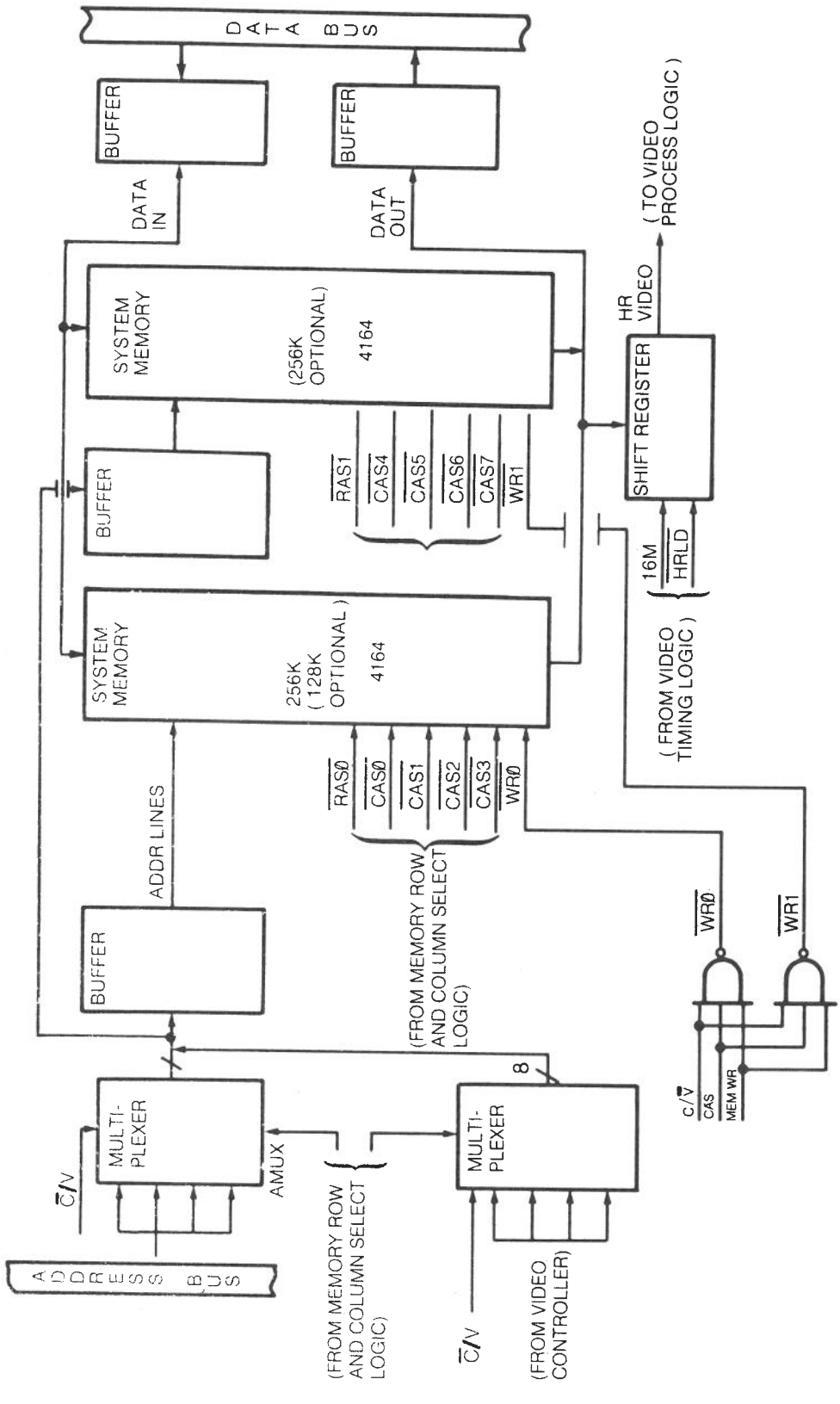


Fig. 2-14. System memory inputs, outputs, buses and buffers

SERIAL PORT

The 825Ø Universal Asynchronous Receiver-Transmitter (UART) receives serial data from a serial port, converts it to parallel data, and sends it to the CPU. It also converts parallel data from the CPU to serial data and sends it to a serial port. The UART communicates with the CPU through data buffers. Figure 2-15 is the block diagram for the UART showing the logic for both serial and parallel ports.

The 825Ø UART generates and receives all the control signals necessary to communicate with a standard RS-232C port. A 1.843 MHz crystal oscillator connected to the UART is divided down and used as the transmission clock.

EIA 12-volt levels are generated for the RS-232 interface. A shorting jumper is used to configure the port as a modem interface for Data Communications Equipment (DCE) or as a printer interface for Data Terminal Equipment (DTE).

When a device connected to the serial port needs to be serviced, the UART sends an Interrupt ReQuest signal (IRQ4) to the 8Ø88 CPU through the interrupt controller.

PARALLEL PORT

The parallel output port logic (Fig. 2-15) enables the CPU to send parallel data to an external peripheral device such as a printer. A data buffer is connected by latches selected by an address decoder and gates. The latch sends the data bits via the parallel port to the external peripheral device.

Handshaking signals from the CPU are latched and sent to inverters connected to the video controller. The inverters receive handshaking signals from the parallel port, which are latched and sent to the CPU through a buffer. An Interrupt ReQuest signal (IRQ7) is generated and sent through inverters to the interrupt controller.

FLOPPY DISK CONTROLLER

The 8272 Floppy Disk Controller (FDC) enables the computer to control one or two double-sided, double-density disk drives. Data can be read or written at a speed of 25ØK bits per second using a Modified Frequency Modulation (MFM) recording format. The 8272 FDC receives and transmits data through a bidirectional buffer to the system data bus. The data lines are connected directly to the FDC and also the Floppy Disk Drive (FDD) selection logic. Figure 2-16 is the block diagram for the Floppy Disk Controller.

The 8272 FDC is enabled by a select signal from the FDC address logic, which also controls the direction of data transfer through the data buffer. The FDC operates in a DMA mode for transferring information to or from the disk by generating a DMA request for each byte to be transferred. When the operation is completed, the FDC sends an interrupt request to the CPU.

Data is written onto the disk through write precompensation circuitry, and read from the disk with assistance from a phase-lock loop data separator. Control of the disk drives is accomplished by means of the head position and drive control logic, and the disk drive selection logic.

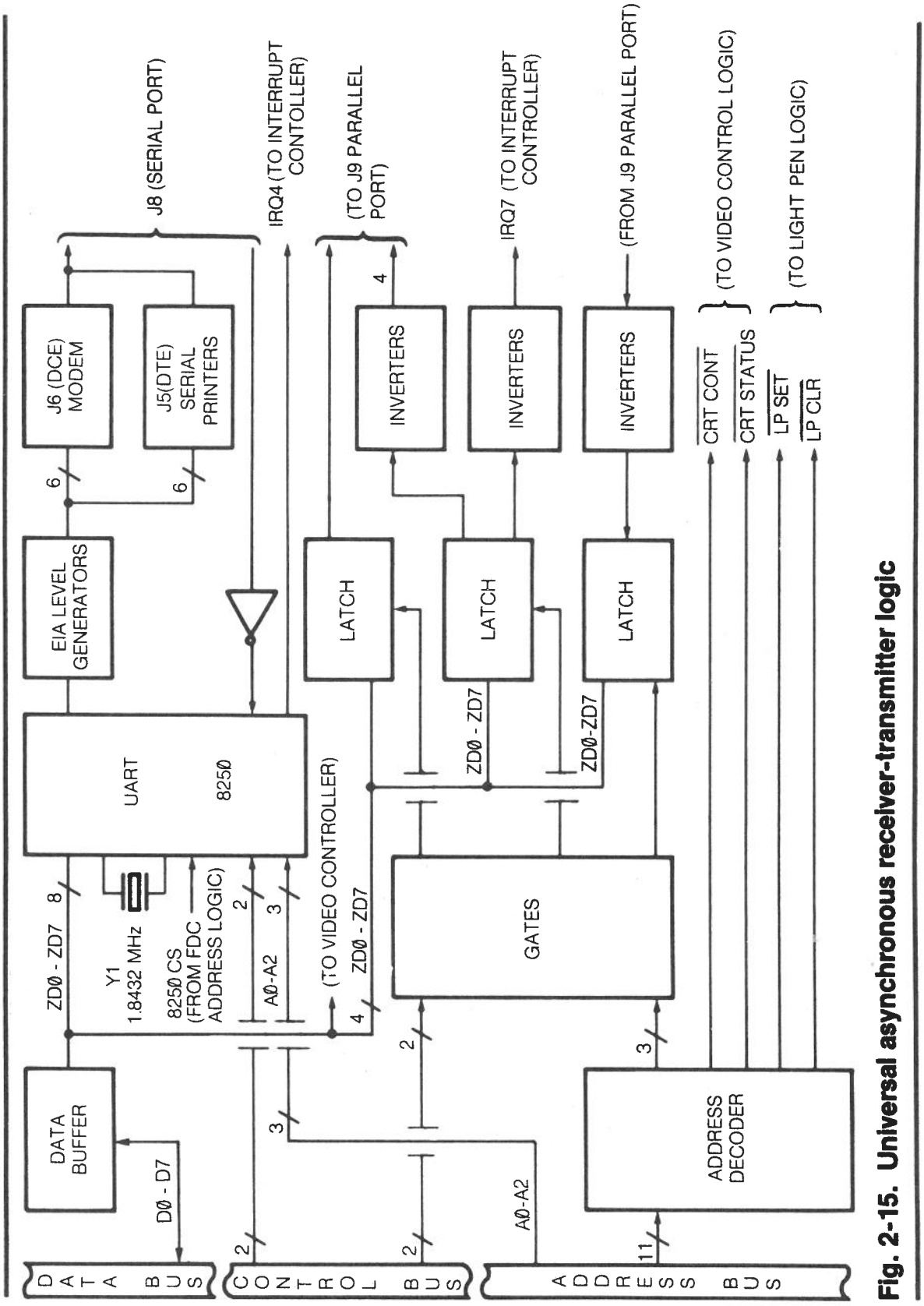


Fig. 2-15. Universal asynchronous receiver-transmitter logic

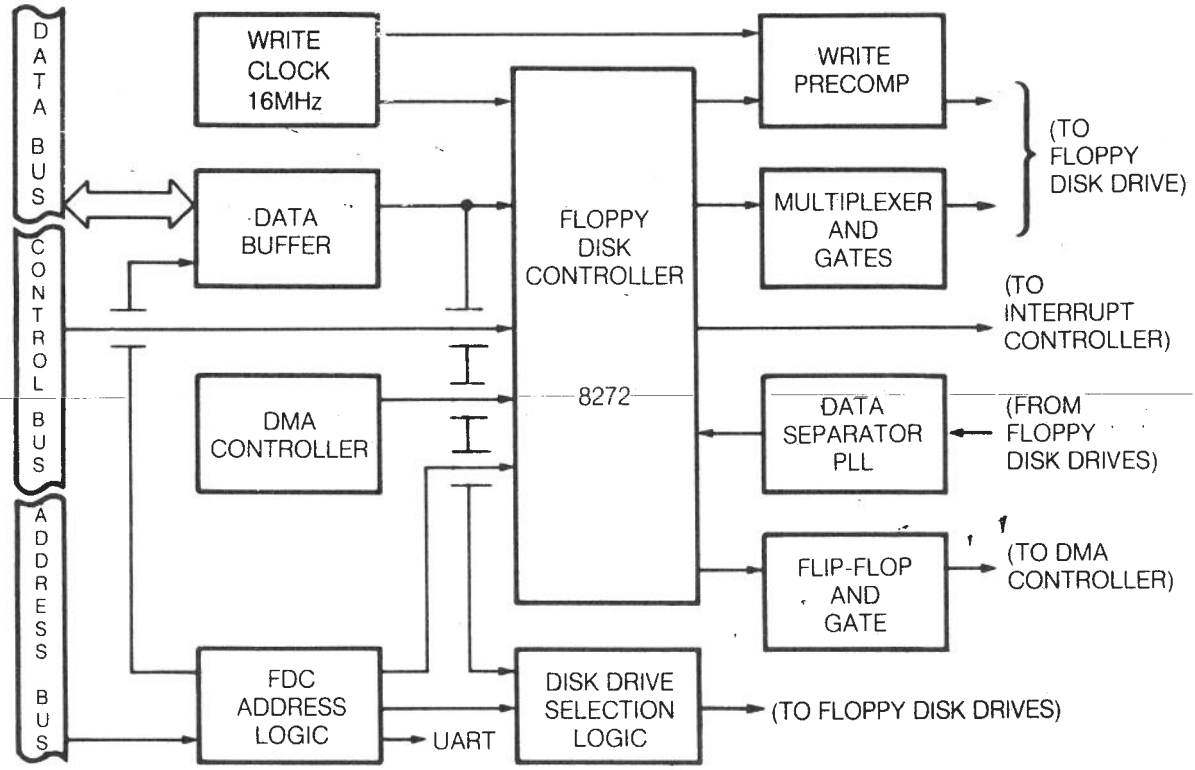


Fig. 2-16. Floppy disk controller

Timing signals for the FDC and Write PreCompensation (WPC) logic come from the write clock, a 16-MHz crystal with frequency dividers. Write precompensation specifies the exact position for each bit on the disk. It avoids reading problems that would result from variations between disk drives.

The FDC has logic to control selection of read/write, disk drive, and side 0 or side 1 read/write head. The drive motor is activated approximately 0.5 seconds before a read/write operation is to take place to enable the disk to reach a stable speed before data is transferred. The timing relationships for reading data from or writing data to a floppy disk are shown in Fig. 2-17.

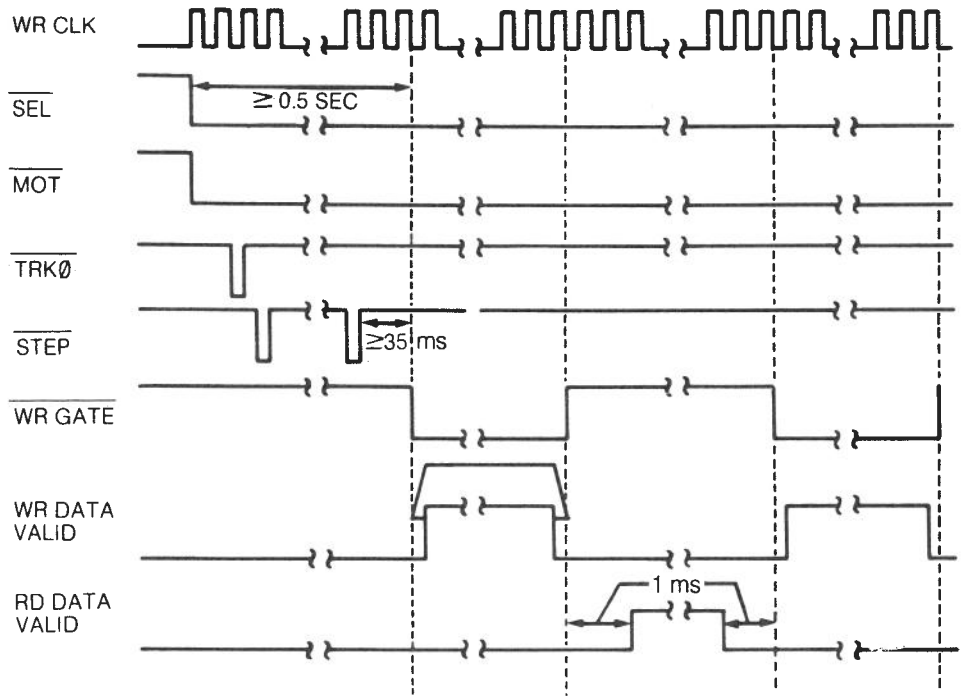


Fig. 2-17. Read-write data signals and timing

PERSONAL HARD DISK

The Personal Hard Disk (PHD) unit facilitates rapid access to 10 Megabytes of storage. Two versions of the hard disk drive are available: one mounted in the system unit, and one external to the system unit. For the internal PHD, the disk controller module port select function is integrated with the interface card. This section discusses only the internal PHD .

Disk Controller Module

The Disk Controller Module (DCM), which resides between the hard disk interface card and the disk drive, has the following functions:

- Provides access ports through which the system software controls the disk drive.
- Provides the data and status interface between the disk drives and the system.
- Calculates sector number and boundaries with respect to the index pulse from the drive without reading physical addresses from the disk.
- Provides on-board RAM buffer memory for data transfer both to and from the disk.
- Provides an Error Checking and Correction (ECC) code that is written on the disk, and read back as a data validity check.

- Serializes and de-serializes data to and from the disk drive.
- During a READ operation, derives separate clock and data streams from the MFM encoded data on the disk.
- Provides write precompensation based on serial bit pattern of the MFM encoded WRITE data.

Port Selection

For the external PHD, address lines A1, A2, along with Signal INPut ($\overline{SINP}$) and Signal OUTput ($\overline{SOUT}$) are input from the system interface board in the computer. The internal PHD integrates the port select function with the system interface. Data lines DØ-D7 are bidirectional and are controlled by the data bus buffer logic.

Figure 2-18 shows the disk controller module block diagram for the internal PHD. The port select logic outputs ReaD commands $\overline{RD0}$-$\overline{RD3}$ and WRite commands $\overline{WR0}$-$\overline{WR3}$. The disc controller module decodes these ports. RD1 is not used.

Disk-Read Operation

The following parameters must be set up for a disk-read operation to take place:

- The sector number to access is selected, disk read is selected, Error Checking and Correction (ECC) code is either enabled or disabled, and Write PreCompensation (WPC) is either enabled or disabled. These functions are all accomplished by writing to DCM port 1.
- The proper disk drive is selected, the head is selected, the drive is stepped in or out to the desired track, and low current write is enabled or disabled depending on the head-to-track position. These functions are enabled with a write to DCM port Ø.
- Once the disk head is located at the selected track, a write to port 3 is done to start the read process.

Sector Seek Operation

The sector being sought is latched and applied to one side of a 6-bit comparator. When the other side of the comparator matches the inputs, SECTOR MATCH and $\overline{SECTOR\ MATCH}$ are both true, and a latch is set. Figure 2-19 is a block diagram of the internal DCM sector counter.

Inputs SØ' and S4' are supplied by a frequency synthesizer circuit. An integrated Phase-Lock Loop (PLL) circuit receives a buffered INDEX signal from the disk drive. This input occurs every 16.67 ms. Since a track contains 32 sectors (Ø-31), the clock increments the divide-by-16 counters to provide 32 distinct counts as SØ'-S4' every revolution of the disk or every 16.67 ms.

A resistor-capacitor network provides a signal of approximately 15 KHz which is input as a clock. Flip-flops reduce this to approximately 1920 Hz, which is double the frequency of outputs SØ'-S4'. This match in signal frequencies is essential to keep the circuit in lock.

If a loss of lock occurs, a one-shot "loss of sync" pulse is applied to the data bus on DB5. As long as the circuit stays in lock, SØ' to S4' are counting from Ø to 31 between each occurrence of the INDEX pulse from the disk drive. When SØ to S4 matches SØ' to S4', a true SECTOR MATCH signal confirms that the drive head is located over the correct sector.

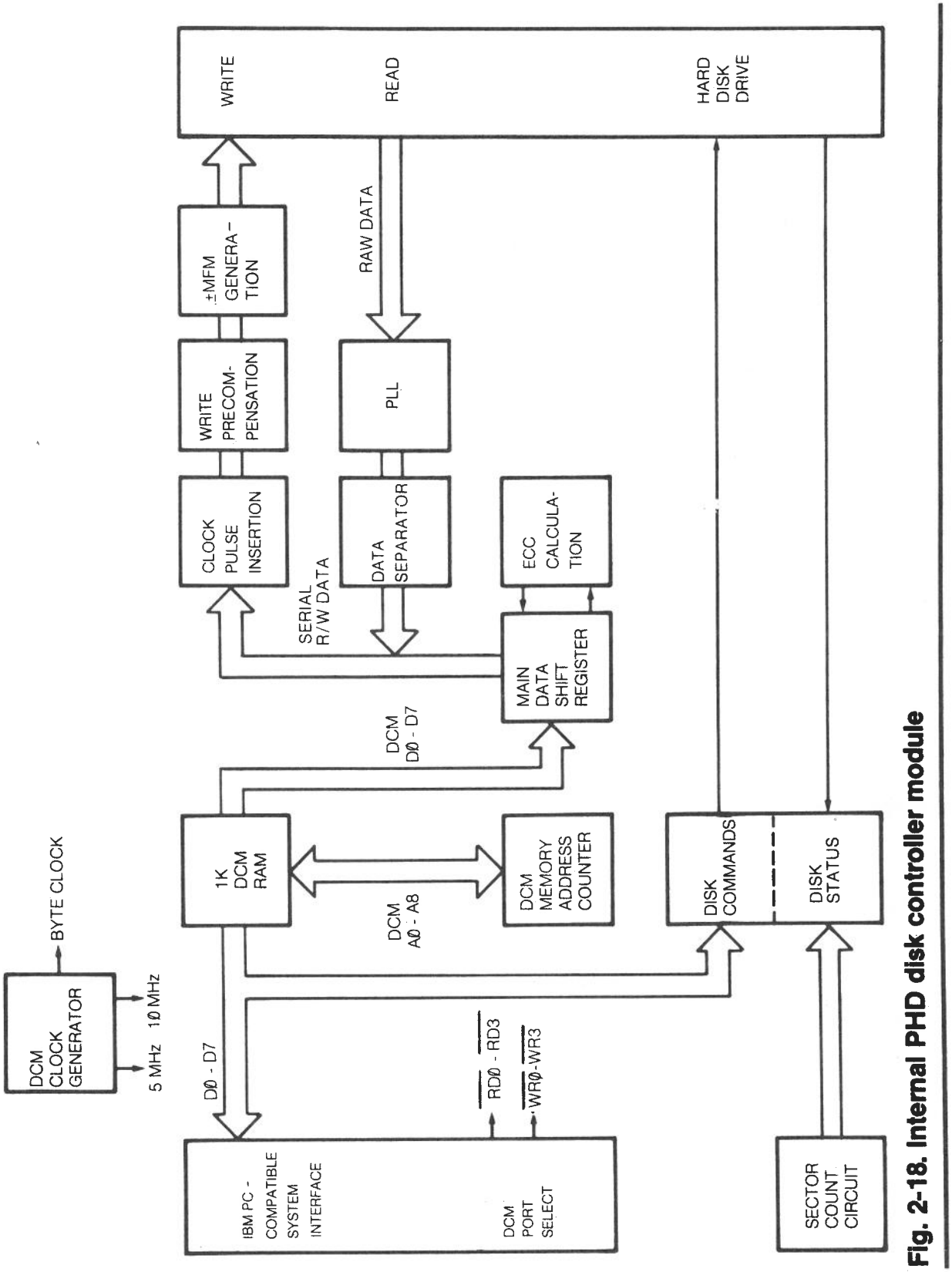


Fig. 2-18. Internal PHD disk controller module

When SECTOR MATCH is true, the controller is no longer in a cleared state, and so it starts counting the equivalent of an 8-bit or 1-byte period called BYTE CLOCK. This signal is based on a 5-MHz bit clock rate, which is the data transfer rate of the disk drive.

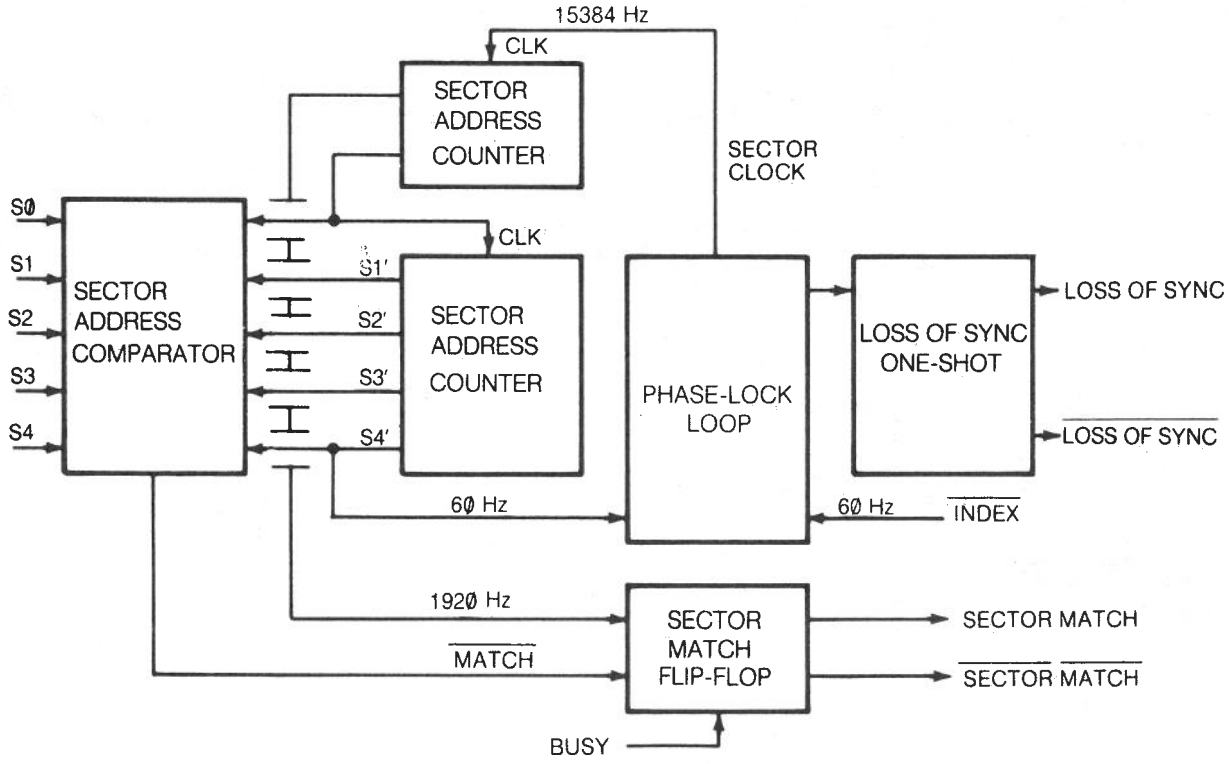


Fig. 2-19. Sector counter for internal PHD

Memory Enable to Read Disk Data to DCM RAM

When BYTE CLOCK is true, the RAM Chip Select (RAM $\overline{CS}$) inputs become active. The falling edge of BYTE CLOCK increments the memory address after each byte of data is transferred from the drive to the disk controller module. As BYTE CLOCK goes high in coincidence with disk read, the signal $\overline{RD}$ $\overline{CK}$ becomes active low. This provides an active RAM $\overline{WR}$ signal. Figure 2-20 shows the memory data transfer for the internal PHD.

Data Read From Disk to Memory

Data and clock pulses are now transferring from the disk at 5M bits/sec. This data is processed to be Transistor-Transistor Logic (TTL) compatible. The raw read data, which contains data and clock pulses, is applied to two areas.

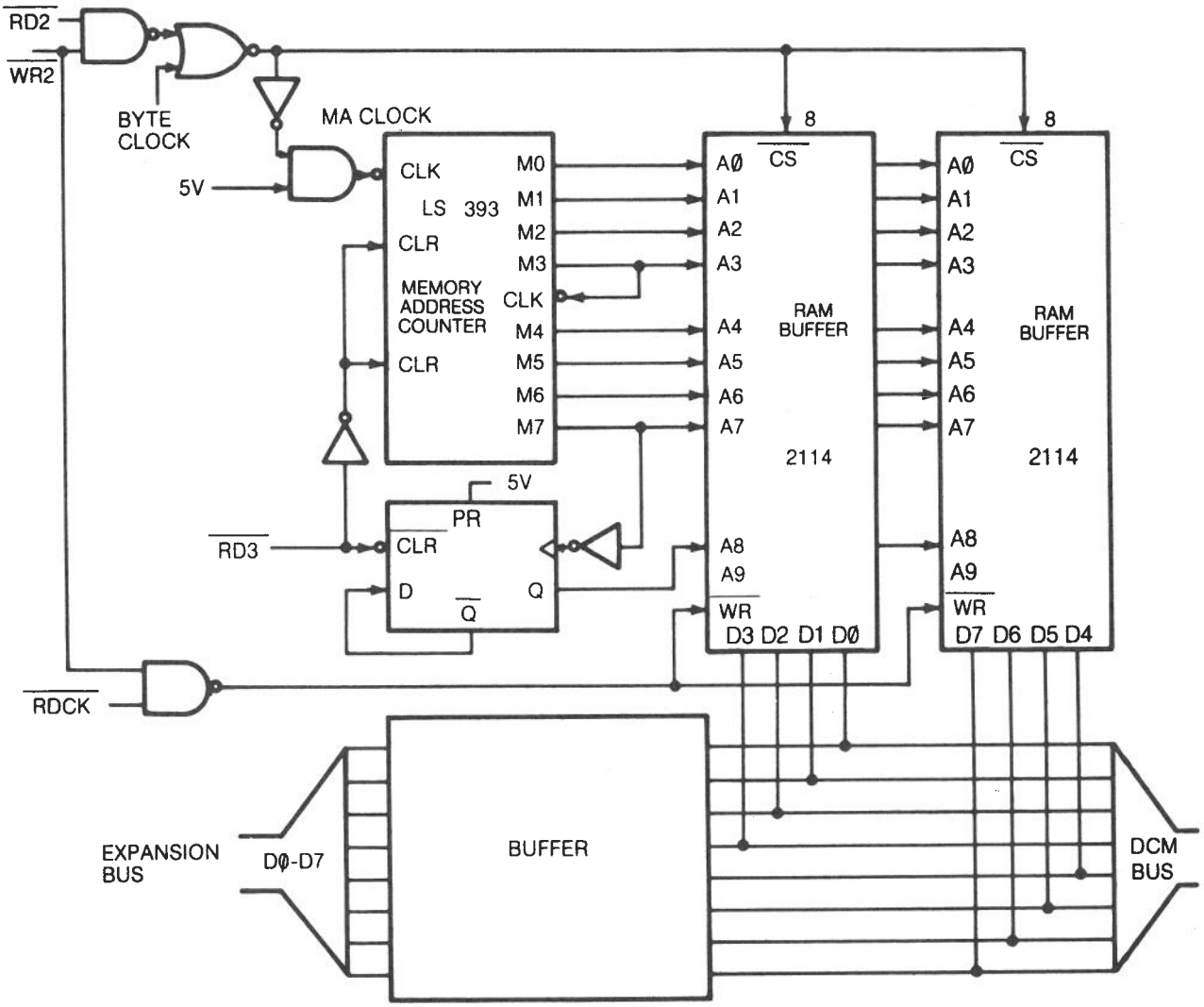


Fig. 2-20. Memory data transfer for internal PHD

Raw data is applied to a phase comparator section of the Phase-Lock Loop (PLL) circuit. The raw data frequency is compared to the Voltage Controlled Oscillator (VCO) output. Any phase difference will result in a voltage being applied to the V1 input of the VCO circuit. This difference in voltage will either speed up or slow down the VCO circuit. The output of the VCO circuit serves as a clock for the data separator circuit.

Raw data is also applied to a clock/data separator circuit. Basically, the 10-MHz VCO clock is divided in two to provide a bit clock signal. The pulse is treated as a clock pulse and is stripped if a raw data pulse occurs during a low bit clock or if a rising edge signal coincides with a rising edge bit clock.

The read data output of the separator is transferred to a shift register because the Error Check and Correction TIME (ECC TIME) is also low, and because of the following configuration inputs:

WRITE GATE and BYTE CLOCK are low.

$\overline{RD}$ $\overline{CK}$ is high.

Clear (C) of the Shift Right Data Read circuit is high.

The shift right register is enabled with its data bus I/O lines tri-stated. Read Data (RD) causes the register to shift 8 bits of data in, and BYTE COUNT goes active. This drives the data bus I/O lines out of tri-state, allowing data in the register to be output on the bus and written into memory. Since the toggling of BYTE CLOCK increments the memory address pointer, each assembled byte is stored one location higher than the previous byte.

Error Check and Correction Action During Disk Read

While READ DATA is being applied to the main data shift register (Fig. 2-18), it is also being applied to a parity generator that takes READ DATA from four shift registers and creates an odd or even parity signal depending on the bits applied. This signal is then fed back into the shift registers.

After all 256 bytes are read, ECC shift registers contain a unique code derived from the values of the 256 bytes plus the outputs of X0-X24.

At count 256 a PROM makes output Q1 active for four counts, or 32-bit clocks. This causes both ECC TIME signals to become active. Note that $\overline{ECC}$ $\overline{TIME}$ causes a shifting of data only. Inputs from the parity generator will not be added to the values of the ECC shift registers.

At the end of 260 bytes of transfer, $\overline{ECC}$ $\overline{TIME}$ signals are turned off. At this point, the head of the disk drive is now over the postamble of the current sector, which is all zeros. The sector timing circuit has incremented the count past the matching sector values, and so the sector match signal is turned off. With SECTOR MATCH inactive, BYTE CLOCK ceases. With BYTE CLOCK inactive, the memory address counter remains unchanged.

ECC Summary

Error Check and Correction (ECC) is calculated on the 256 bytes of data read from the disk. The code is generated on odd parity outputs resulting from the serial read data and the outputs of the ECC. This code differs from normal Cyclic Redundancy Check (CRC) in that ECC allows software to find and correct the fault.

ECC is generated during a write to the disk and is written as 4 bytes after the 256 data bytes in the sector. During read back, the 4-byte ECC code is recalculated from the read data. If the result is non-zero, an error has occurred.

Read Delay

The read delay network is responsible for synchronizing the data separation bit clock to the sync bytes read from the inner sector gaps of the disk.

The counter counts up to 128 clock bits after SECTOR MATCH becomes true and then makes $\overline{\text{READ DELAY}}$ active. This signal is NANDed with RD and VCO CLK to place the head of the drive in the midst of the sync gap after the initial 128 bit clock time period. The $\overline{\text{READ DELAY}}$ signal causes the BYTE CLOCK to be synchronized with the RD information being transferred from the disk.

Disk Write Operation

As with the disk-read operation, certain requirements must be met before an actual write operation can take place. The following lists the essential prerequisites:

- DCM memory has to be loaded with the 256 bytes of data to be written to the disk.
- ECC shift register must be cleared with a read of DCM port 3.
- The head must be positioned at the proper track, the head must be selected, and the drive must be selected. This is accomplished with a write to DCM port Ø.
- The sector number to write is selected, disk write is selected, ECC is enabled, and write precompensation is selected as necessary. This is accomplished with a write to port 1.
- A write to port 3 is done to start the disk function.

Once port 3 is written to, BUSY becomes active just as it did during a read process. When SECTOR MATCH signals become true, $\overline{\text{SECTOR MATCH}}$ and $\overline{\text{WR}}$ are NORed to provide a high WRITE GATE. This signal is further NANDed with the loss of index to sector counter sync signal $\overline{\text{LOS}}$. If $\overline{\text{LOS}}$ is inactive, which is the normal state, WRITE GATE becomes active, enabling the write circuitry in the disk drive.

DCM Memory to Shift Register Data Transfer

With WRITE GATE and BYTE COUNT both active, a byte from memory is loaded into the shift register. Memory ICs are enabled just as they were during the read process. Chip Select ($\overline{\text{CS}}$) is active because BYTE CLOCK is active. $\overline{\text{WR}}$ is inactive, however, because ReaD ClocK ($\overline{\text{RD CK}}$) is inactive. The memory address counter is incrementing just as it did during a read operation.

Data Serialization

With the data register loaded, the bit clock will serially clock the data transfer. ECC TIME is inactive at this time, which causes serial data to be clocked out as SR DATA.

Write Precompensation, Clock Insertion, and Data Offset

The Shift Register DATA (SR DATA) signal activates:

- A write precompensation PROM, which compares the data outputs for particular data patterns. If Write PreCompensation (WPC) is active, outputs Q0-Q2 cause the data pulses to occur 12 ns early, 12 ns late, or "on time."
- A clock insertion network, which is responsible for insertion of clock pulses in the data stream as required by MFM rules.

ECC Write to Disk

ECC calculation is the same as it was during the read process. However, with $\overline{WR}$ active, the serial shift data is clocked out just as with READ DATA.

At the end of 256 bytes of data, an ECC is present in the ECC counter, and ECC TIME signals are active. When ECC TIME is true, the ECC data is clocked and is written to the disk.

When BYTE CLOCK is active, ECC TIME signals become inactive. Thus, no data is loaded, and the ECC does not recalculate its own value.

I/O INTERFACES

The Input/Output (I/O) channel enables peripheral devices to be interfaced with the CPU. Interface logic for the serial and parallel ports, floppy disk drives, and monitor is integrated with the PC main board. Four expansion slots extend the system capabilities. The I/O channel uses an 8-bit bidirectional data bus. It has clock and timing lines, three DMA channels, control lines for memory and I/O read or write, and six levels of interrupt.

Section 3
SYSTEM INPUTS AND OUTPUTS

A number of input, output, and input/output (I/O) devices can be operated in conjunction with the Personal Computers (PC). Standard options have been integrated into the main PC board, and additional options can be incorporated using the four I/O expansion slots.

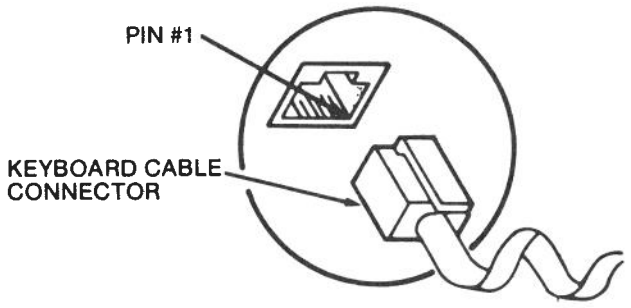
Additional memory as an expansion option is not normally required because the PC provides for up to 512K of memory on the main board. High-resolution graphics are also provided. I/O interfaces that are integral to the main PC board support:

- The keyboard.
- The super-resolution video monitor.
- Serial communication devices.
- Parallel communication devices.

The expansion slots can be used for color graphics, a modem, or other additional features determined by the user.

THE KEYBOARD

The keyboard is connected to the front of the system unit by a six-foot coiled cable with telephone type mini-plugs at each end. The shielded cable has six wires: +5 vdc, ground, clock, data, reset, and DC return lines. The keyboard uses capacitance switching to ensure reliable operation. Figure 3-1 shows the mini-plug connectors.



PIN	SIGNAL
1	GROUND
2	CLOCK
3	DATA
4	$\overline{\text{RESET}}$
5	+ 5 VDC
6	DC RETURN

Fig. 3-1. Mini-plug connector for keyboard

The Keyboard

The keyboard includes a standard typewriter keyboard, 10 function keys, a numeric keypad, and keys for special computer operations. Keyboard functions are controlled by system software, enabling the function keys and numeric keypad to have unique functions for different programs.

Alphanumeric keys are programmed for repeat key action. When held down for a certain length of time, key-press signals are sent at regular intervals. Alternative keyboard functions are produced using Shift, Ctrl, and Alt. Toggle keys include Num Lock, Scroll Lock, and Caps Lock. Keys used for data entry include Escape, Insert, Delete, Space, Backspace, Tab, ←, ↑, Return, and Enter.

The keyboard has an Intel 8048 microprocessor that scans the keyboard and generates a scan code. It communicates with the system via a bidirectional serial interface with a handshake protocol. The scan code is not ASCII code. It is a numeric code (1 through 83) assigned to adjacent typewriter keys, function keys, and numeric keypad. When a key is pressed, the scan code is sent to the system unit. When the key is released, a break code (scan code plus 128 (Hex 80)) is sent to the system unit.

Figure 3-2 is a block diagram of the keyboard circuitry. Keyboard actions are communicated to the system unit using interrupts and ports. The interrupts activate ROM BIOS routines. These routines read the scan code from the keyboard port. This signals the keyboard to clear the key action from its buffer. In the event that the system is unable to respond to the interrupt, the scan code is stored in the keyboard buffer. The 8048 keyboard microprocessor can buffer up to 20 keystrokes.

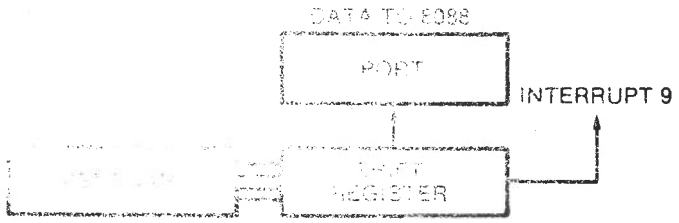


Fig. 3-2. Keyboard Interface

The ROM BIOS monitors the status of shift and toggle keys, and determines legal combinations of shifted keys. Appendix B shows the keyboard scan codes and functions for each key used singly, and when combined with shift functions Shift, Ctrl, or Alt. The only legal combination of three keys is Ctrl-Alt-Delete, which stops all operations and reboots the system.

SUPER-RESOLUTION VIDEO MONITOR

The video monitor with specifications in Table 3-1 achieves full resolution for the super-resolution characters and graphics.

Table 3-1
CHARACTERISTICS OF SUPER-RESOLUTION VIDEO MONITOR

ITEM	SPECIFICATION
Video Signal	
bandwidth	17.185 MHz
horizontal drive	21.Ø6 KHz
screen refresh	6ØHz
Screen	
nonglare surface	
P31 green or amber phosphor	
Characters	
each line	8Ø characters
number of lines	25 lines
character box:	16 pixels wide
	13 pixels high
character size:	12 pixels wide
	9 pixels high
Character Attributes	
normal	
underline	
high intensity	
inverse	
flashing	
Graphic Resolution	
horizontal	64Ø pixels
vertical	325 pixels

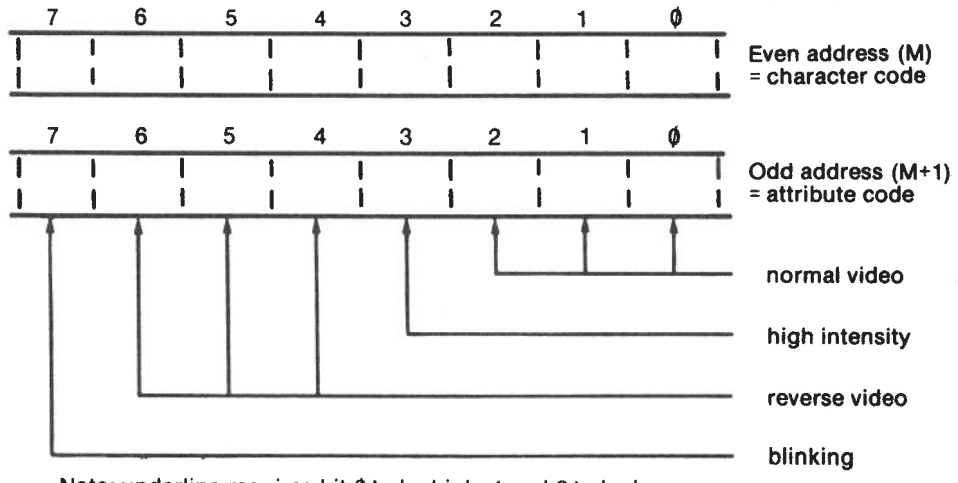
Programming Considerations

Proper initialization of the 6845 video controller after power-on or reset is essential to avoid equipment damage. Table 3-2 lists the values that must be programmed into the 6845 registers. The initial command to port 3B8, Hex Ø1, sets the high-resolution mode. Otherwise, the CPU would be in a wait state of indeterminate length.

Table 3-2
INITIALIZATION OF 6845 VIDEO CONTROLLER

REGISTER	REGISTER FILE	FUNCTION	VALUE
RØ	Horizontal total	Characters	65H
R1	Horizontal displayed	Characters	5ØH
R2	HSYNC position	Characters	51H
R3	HSYNC width	Characters	ØAH
R4	Vertical total	Character rows	1AH
R5	VTOTAL adjust	Scan line	ØØH
R6	Vertical displayed	Character row	19H
R7	VSYNC position	Character row	19H
R8	Interface mode	———	Ø2H
R9	Max. scan line address	Scan line	ØCH
R1Ø	Cursor start	Scan line	ØAH
R11	Cursor end	Scan line	ØBH
R12	Start address (H)	———	ØØH
R13	Start address (L)	———	ØØH
R14	Cursor (H)	———	ØØH
R15	Cursor (L)	———	ØØH
R16	Reserved		
R17	Reserved		

The display buffer uses an even address for the character code, and an odd address for the character attribute. Figure 3-3 shows the addresses with attribute codes and functions.



Note: underline requires bit Ø to be high; 1 and 2 to be low

Fig. 3-3. Character code and attribute code display buffers

These attributes can be combined in various ways as shown in Table 3-3.

Table 3-3
COMBINATION OF VIDEO ATTRIBUTES

BIT 7	6	5	4	3	2	1	0	FUNCTION
0	0	0	0	0	0	0	0	Non display
0	1	1	1	0	0	0	0	Reverse video
0	0	0	0	0	1	1	1	Normal video
0	0	0	0	1	1	1	1	High intensity normal video
0	1	1	1	1	0	0	0	High intensity reverse video
1	0	0	0	0	1	1	1	Blinking normal video
1	1	1	1	0	0	0	0	Blinking reverse video
0	0	0	0	0	0	0	1	Underline normal video
0	1	1	1	0	0	0	1	Underline reverse video
1	0	0	0	0	0	0	0	Blinking underline normal video
1	1	1	1	0	0	0	1	Blinking underline reverse video

The monitor interface accepts 256 character codes. An 8K character generator ROM contains the fonts, block graphics, and character codes used in the screen display. A table of character sets and character codes is presented in Appendix E.

The character display buffer supports one screen of 80 times 25, or 2000 characters, plus a character attribute for each character displayed. The display buffer has 4K bytes of memory, and no system RAM is required. The buffer starts at B0000H.

Table 3-4 shows the I/O addresses and bit map used to program the 6845 video controller. The index and data registers interface the controller with the super-resolution video display.

Table 3-4
I/O ADDRESSES AND BIT MAP

I/O REGISTER	FUNCTION	I/O REGISTER	FUNCTION
3B0H	Not used	3B8H	Video control port 1
3B1H	Not used	3B9H	Reserved
3B2H	Not used	3BAH	Video status port
3B3H	Not used	3BBH	Reserved
3B4H	6845 index register	3BCH	Parallel data port
3B5H	6845 data register	3BDH	Printer status port
3B6H	Not used	3BEH	Printer control port
3B7H	Not used	3BFH	Not used

Table 3-5 shows the bit assignment for the control port and the status port.

Table 3-5
6845 VIDEO MONITOR CONTROL PORT (3B8 HEX)
AND STATUS PORT (3BA HEX)

CONTROL PORT (3B8H)		STATUS PORT (3BAH)	
BIT NUMBER	FUNCTION	BIT NUMBER	FUNCTION
Ø	Not used	Ø	Horizontal drive
1	Not used	1	Reserved
2	Not used	2	Reserved
3	Enable alphanumeric	3	Black/white video
4	Not used		
5	Enable blink		
6	Not used		
7	Enable super-resolution graphics		

PARALLEL PORT

The parallel interface is part of the main PCB, and can be used for any application that matches its input/output capabilities. It has 12 Transistor-Transistor Logic (TTL) buffer outputs which are latched, and can be read and written under program control.

One input can be programmed to create a processor interrupt. A reset function is provided.

When the interface is used to attach a printer, the strobe line is activated. Data and commands are loaded into an 8-bit, latched, output port. As data is written to the printer, the program reads the input port for printer status enabling the next character to be written.

The parallel interface responds to five I/O instructions. Two output instructions transfer data into two latches that output to the printer, and two input instructions allow the printer to read back the contents of the two latches. A third input is used by the processor to read the real-time status of a group of connector pins. Table 3-6 describes these output and input functions.

ASYNCHRONOUS COMMUNICATIONS (SERIAL) INTERFACE

This interface can be programmed to support any asynchronous communications device. It will add or remove start, stop, or parity bits. The baud-rate generator can be programmed for rates from 50 to 9600 baud. Characters may be 5, 6, 7, or 8 bits with 1, 1-1/2, or 2 stop bits. The prioritized system of interrupts controls transmit, receive, error, line status, and data set interrupts. Loopback functions of transmit/receive and input/output signals can be used for diagnostic purposes.

Table 3-6
PARALLEL INTERFACE:
INPUT AND OUTPUT ADDRESSES AND PIN NUMBERS

I/O INSTRUCTIONS

Input from address **Hex 3BC**
Input from address **Hex 3BD**

Output to address **Hex 3BC**

bit number:	7	6	5	4	3	2	1	0
read from pin number:	9	8	7	6				

Output to address **Hex 3BE**
Signal IRQ enable (bit 4)

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0

Real-time status to processor

bit number:	7	6	5	4	3	2	1	0
read from pin number:	11	10	12	13	15			

Additional features include:

- Double buffering to reduce synchronization problems.
- Independent clock input from receiver.
- Modem control functions.
- False start bit detection.
- Line break generation and protection.

The communications protocol is a function of the system microcode. It must be loaded before the interface is operational. System software is required to pace the interface and control signal status. The required mode of operation is determined by programming the 8250 asynchronous communications element.

Bit 3 of the modem control register must be set high (1) for the communications logic to send interrupts to the system. This will cause any interrupt allowed by the interrupt enable register to be implemented. Figure 3-4 shows the data format.

The interface has a 25-pin, D-shell, female connector, and is EIA RS-232C compatible.

The voltage serial interface supports the data and control signals listed in Table 3-7. The interface converts signals to and from TTL levels to EIA voltage levels. These signals are interpreted or generated by the 8250 asynchronous communications element.

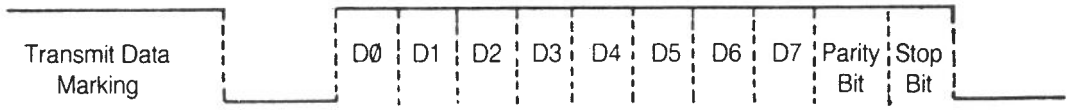


Fig. 3-4. Communications interface data format

Table 3-7
ADDRESS BITS FOR SERIAL COMMUNICATIONS
(Hex Address 3F8 to 3FF and 2F8 to 2FF)

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DLAB	REGISTER
1	1/Ø*	1	1	1	1	1	X	X	X	Ø	Receiver Buffer READ Transmit
							Ø	Ø	Ø	Ø	Holding Register WRITE
							Ø	Ø	1	Ø	Interrupt Enable
							Ø	1	Ø	X	Interrupt Identify
							Ø	1	1	X	Line Control
							1	Ø	Ø	X	Modem Control
							1	Ø	1	X	Line Status
							1	1	Ø	X	Modem Status
							1	1	1	X	None
							Ø	Ø	Ø	1	Divisor Latch (LSB)
							Ø	Ø	1	1	Divisor Latch (MSB)

*Note: Bit 8 is logical 1 for primary interface and logical Ø for secondary interface.

Table 3-8 lists the addresses for the input/output (I/O) registers which are accessible through the I/O channel.

Table 3-8
I/O DECODES IN HEX

PCB INTERFACE	I/O SLOT	REGISTER	DLAB STATE
3F8	2F8	TX Buffer	DLAB = Ø(WRITE)
3F8	2F8	RX Buffer	DLAB = Ø(READ)
3F8	2F8	Divisor Latch LSB	DLAB = 1
3F9	2F9	Divisor Latch MSB	DLAB = 1
3F9	2F9	Interrupt Enable Register	
3FA	2FA	Interrupt Identification Register	
3FB	2FB	Line Control Register	
3FC	2FC	Modem Control Register	
3FD	2FD	Line Status Register	
3FE	2FE	Modem Status Register	

The signal is in the marking condition when voltage at the interface is more negative than -3 volts, and in the spacing condition when positive voltage exceeds 3 volts. The transition region between +3 and -3 volts is invalid, and signals outside the range of -15 volts to +15 volts are also invalid. At valid signal levels, the interface control function is ON when voltage exceeds +3 volts, and OFF when voltage is more negative than -3 volts.

The program can access or control any of the INS8250 registers through the processor. These registers control INS8250 operations and are used to transmit and receive data. The format of the asynchronous data communications exchange is specified by the programmer through the line control register. Table 3-9 shows the reset controls and states.

Table 3-9
RESET CONTROLS AND STATES

REGISTER OR SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits LOW (Ø-3 forced, 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit Ø is HIGH, Bits 1-2 LOW Bits 3-7 permanently LOW
Line Control Register	Master Reset	All bits LOW
Modem Control Register	Master Reset	All bits LOW
Line Status Register	Master Reset	All bits LOW except Bits 5-6 HIGH
Modem Status Register	Master Reset	Bits Ø-3 LOW Bits 4-7 Input Signal
SOUT	Master Reset	HIGH
INTRPT (RCVR errors)	READ LSR/MR	LOW
INTRPT (RCVR data ready)	READ RBR/MR	LOW
INTRPT (RCVR data ready)	READ IIR WRITE THR WRITE MR	LOW
INTRPT (modem status changes)	READ MSR READ MR	LOW
OUT2	Master Reset	HIGH
Request to send	Master Reset	HIGH
Data Terminal Ready	Master Reset	HIGH
OUT1	Master Reset	HIGH

Accessible Registers

Any of the INS8250 registers may be accessed or controlled through the 8088 Central Processing Unit. These registers are used to control INS8250 operations and to transmit and receive data. They are described in the following sections.

Modem Status Register

This 8-bit register provides the current state of the control lines from the modem (or peripheral device) to the CPU. In addition, four bits of the Modem Status Register (MSR) provide change information. These bits are set to logic 1 whenever a control input from the modem changes state. They are set to logic Ø whenever the CPU reads the MSR. Figure 3-5 describes the data bits for the MSR.

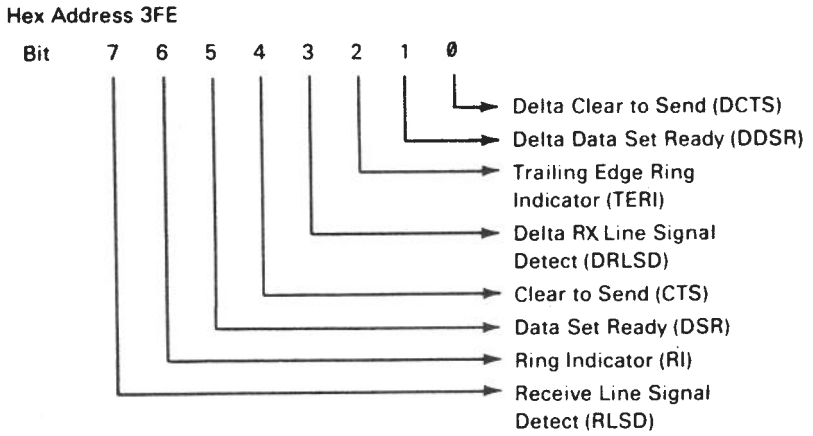

Hex Address 3FE
Bit 7 6 5 4 3 2 1 Ø
Delta Clear to Send (DCTS)
Delta Data Set Ready (DDSR)
Trailing Edge Ring Indicator (TERI)
Delta RX Line Signal Detect (DRLSD)
Clear to Send (CTS)
Data Set Ready (DSR)
Ring Indicator (RI)
Receive Line Signal Detect (RLSD)

Fig. 3-5. Modem Status Register (MSR)

Bit Ø, Delta Clear to Send (DCTS), indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1, Delta Data Set Ready (DDSR), indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2, Trailing Edge of Ring Indicator (TERI), indicates that the RI input to the chip has changed from an ON (logic 1) to an OFF (logic Ø) condition.

Bit 3, Delta Received Line Signal Detect (DRLSD) indicates that the RLSD input to the chip has changed state.

NOTE

Whenever bit Ø, 1, 2, or 3 is set to a logic 1, a modem status interrupt is generated.

Bit 4 is the complement of the Clear to Send (CTS) input. If bit 4 of the Modem Control Register (MCR) is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5 is the complement of the Data Set Ready (DSR) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6 is the complement of the Ring Indicator (RI) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.

Bit 7 is the complement of the Received Line Signal Detect (RLSD) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 of the MCR.

Modem Control Register

Figure 3-6 shows the 8-bit register which controls the interface with the modem or data set (or a peripheral device emulating a modem).

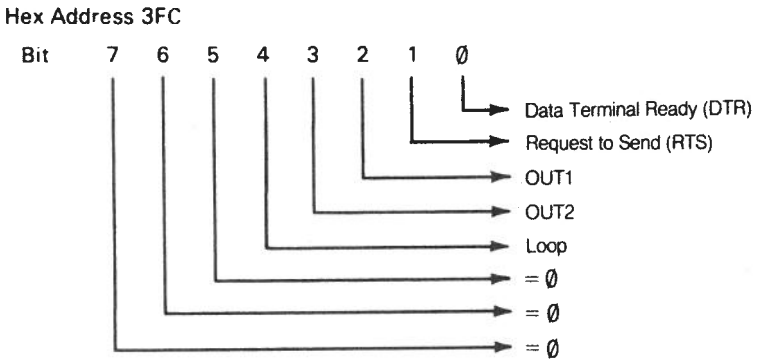


Fig. 3-6. Modem Control Register (MCR)

Bit Ø controls the Data Terminal Ready (DTR) output. When bit Ø is set to a logic 1, the DTR output is forced to logic Ø. When bit Ø is reset to a logic Ø, the DTR output is forced to a logic 1.

NOTE

The DTR output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding modem or data set.

Bit 1 controls the Request to Send (RTS) output. Bit 1 affects the RTS output in a manner identical to that described above for bit Ø.

Bit 2 controls the Output 1 (OUT1) signal, which is an auxiliary user-designated output. Bit 2 affects the OUT1 output in a manner identical to that described above for bit Ø.

Bit 3 controls the Output 2 (OUT2) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT2 output in a manner identical to that described above for bit Ø.

Bit 4 provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following events occur:

- The transmitter Serial OUTput (SOUT) is set to the marking (logic 1) state;

- The receiver Serial INput (SIN) is disconnected;
- The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input;
- The four modem Control inputs (CTS, DSR, RLSD, and RI) are disconnected; and
- The four modem control outputs (DTR, RTS, OUT1, and OUT2) are internally connected to the four modem control inputs.

NOTE

In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register (see Fig. 3-7 below).

The INS8250 interrupt system can be tested by writing into the lower four bits of the Modem Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation, and then bit 4 of the Modem Control Register must be reset to logic 0.

Bits 5 through 7 are permanently set to logic 0.

Interrupt Enable Register

This 8-bit register enables the four types of interrupt of the INS8250 to activate the chip interrupt (INTRPT) output signal separately. It is possible to disable the interrupt system totally by resetting bits 0 through 3 of this register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Figure 3-7 shows the bits of the Interrupt Enable Register (IER).

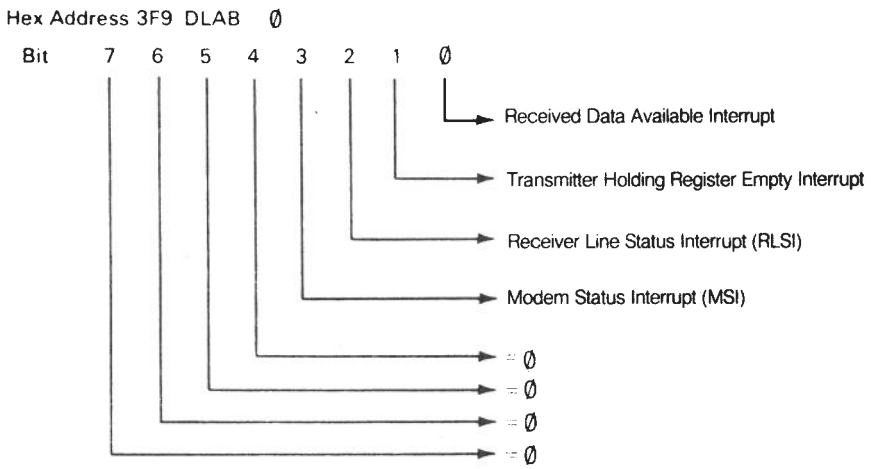

Hex Address 3F9 DLAB 0
Bit 7 6 5 4 3 2 1 0
Received Data Available Interrupt
Transmitter Holding Register Empty Interrupt
Receiver Line Status Interrupt (RLSI)
Modem Status Interrupt (MSI)
= 0
= 0
= 0
= 0

Fig. 3-7. Interrupt Enable Register (IER)

Bit Ø enables the Received Data Available Interrupt when set to logic 1.

Bit 1 enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2 enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3 enables the Modem Status Interrupt when set to logic 1.

Bits 4 through 7 are always logic Ø.

Disabling the interrupt system inhibits the Interrupt Identification Register (see Fig. 3-8) and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

Interrupt Identification Register

The INS8250 has an on-chip interrupt capability that causes minimum software overhead during data character transfers by prioritizing interrupts into four levels. The four levels of interrupt conditions are as follows:

- Receiver Line Status (priority 1);
- Receiver Data Ready (priority 2);
- Transmitter Holding Register Empty (priority 3); and
- Modem Status (priority 4).

These are further detailed in Table 3-10.

The Interrupt Identification Register (IIR) indicates an interrupt is pending and what type it is. This register, when addressed during chip-select time, freezes the highest priority interrupt pending, and no other interrupts are acknowledged until that particular interrupt is serviced by the CPU.

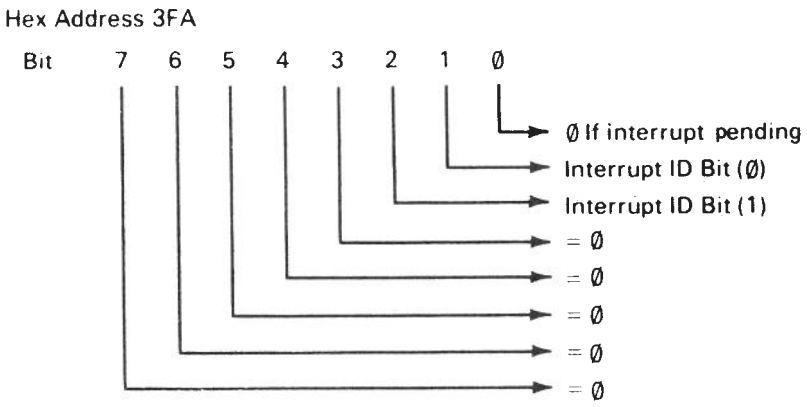


Fig. 3-8. Interrupt Identification Register (IIR)

Bit Ø can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit Ø is a logic Ø, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 1 is a logic 1, no interrupt is pending, and polling (if used) continues.

Bits 1 and 2 are used to identify the highest priority interrupt pending as indicated in Table 3-10.

Bits 3 through 7 are always logic Ø.

Table 3-10
LEVELS OF INTERRUPT CONDITIONS

Interrupt ID Register Bit			Interrupt Set and Reset Functions			
2	1	Ø	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
Ø	Ø	1	—	None	None	—
1	1	Ø	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	Ø	Ø	Second	Receiver Data	Received Data Available	Reading the Receiver Buffer Register
Ø	1	Ø	Third	Transmitter Holding Register	Transmitter Holding Register Empty	Reading IIR Register (if source of interrupt) or writing into Transmitter Holding Register
Ø	Ø	Ø	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

Line Status Register

This 8-bit register provides status information to the CPU concerning data transfer (see Fig.3-9).

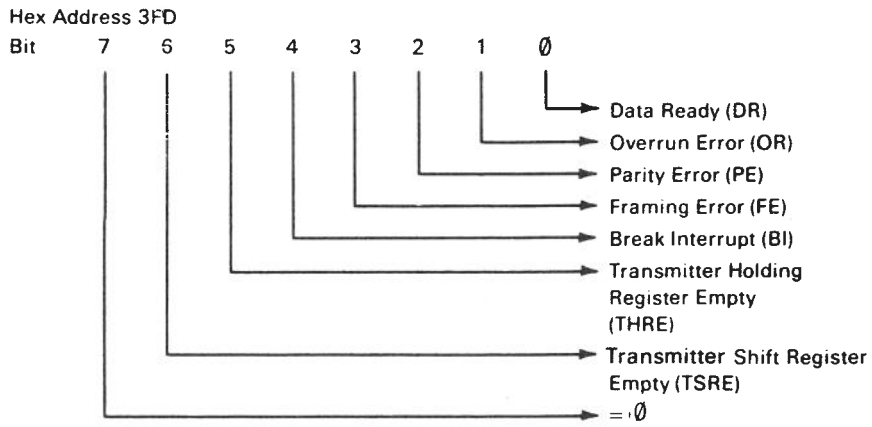


Fig. 3-9. Line Status Register (LSR)

Bit Ø is the receiver Data Ready (DR) indicator. It is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register (see below). Bit Ø may be reset to a logic Ø either by the CPU reading the data in the Receiver Buffer Register, or by writing a logic Ø into it from the CPU.

Bit 1 is the Overrun Error (OE) indicator. It shows that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register. When this happens the previous character is destroyed. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2 is the Parity Error (PE) indicator. It shows that the received data character does not have the correct even or odd parity, as selected by the even parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic Ø whenever the CPU reads the contents of the Line Status Register.

Bit 3 is the Framing Error (FE) indicator. It shows that the received character did not have a valid stop bit. This bit is set to logic 1 whenever the stop bit following the last data or parity bit is detected as a zero bit (spacing level).

Bit 4 is the Break Interrupt (BI) indicator. It is set to a logic 1 whenever the receiver data input is held in the spacing (logic Ø) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5 is the Transmitter Holding Register Empty (THRE) indicator. It shows that the INS8250 is ready to accept a new character for transmission. In addition, it causes the INS8250 to issue an interrupt to the CPU when the Transmitter Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register (see Fig. 3-11 below) into the Transmitter Shift Register. The bit is reset to logic Ø concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6 is the Transmitter Shift Register Empty (TSRE) indicator. It is set to a logic 1 whenever the Transmitter Shift Register is idle. This bit is reset to logic Ø upon a transfer of data from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Receiver Buffer Register

In the Receiver Buffer Register, bit Ø is the least significant bit and is the first bit serially received (see Fig. 3-10).

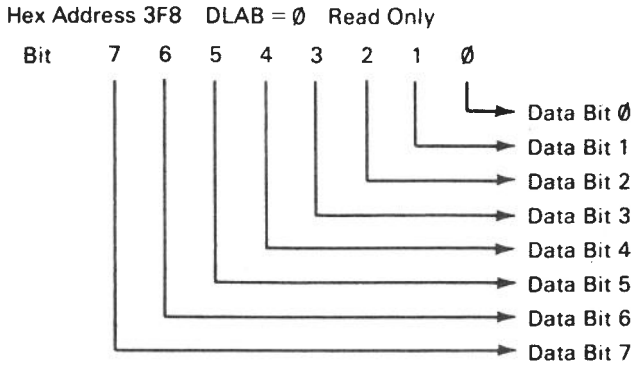

Hex Address 3F8 DLAB = Ø Read Only
Bit 7 6 5 4 3 2 1 Ø
Data Bit Ø
Data Bit 1
Data Bit 2
Data Bit 3
Data Bit 4
Data Bit 5
Data Bit 6
Data Bit 7

Fig. 3-10. Receiver Buffer Register (RBR)

Transmitter Holding Register

In the Transmitter Holding Register (Fig. 3-11), bit Ø is the least significant bit and is the first bit serially transmitted.

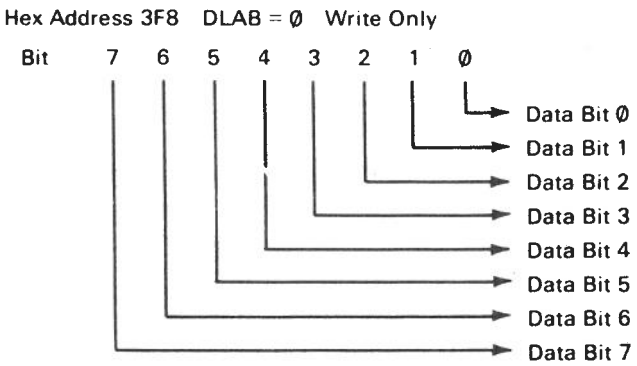

Hex Address 3F8 DLAB = Ø Write Only
Bit 7 6 5 4 3 2 1 Ø
Data Bit Ø
Data Bit 1
Data Bit 2
Data Bit 3
Data Bit 4
Data Bit 5
Data Bit 6
Data Bit 7

Fig. 3-11. Transmitter Holding Register (THR)

Line Control Register

The format of the asynchronous data communications exchange is specified using the Line Control Register. In addition to controlling the format, the contents of this register may be retrieved for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics (see Fig. 3-12).

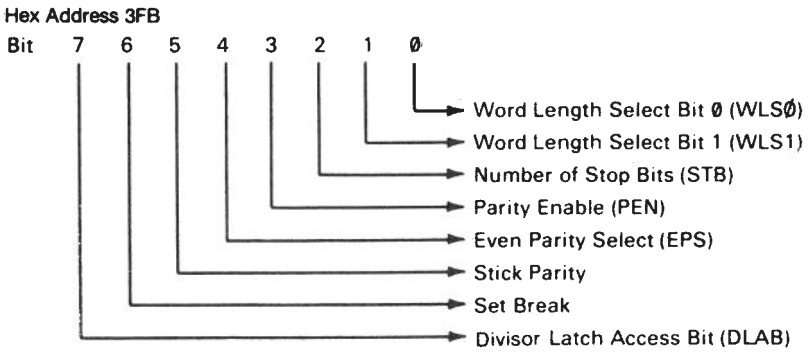

Hex Address 3FB
Bit 7 6 5 4 3 2 1 Ø
Word Length Select Bit Ø (WLSØ)
Word Length Select Bit 1 (WLS1)
Number of Stop Bits (STB)
Parity Enable (PEN)
Even Parity Select (EPS)
Stick Parity
Set Break
Divisor Latch Access Bit (DLAB)

Fig. 3-12. Line Control Register (LCR)

Bits Ø and 1 specify the number of bits in each transmitted or received serial character. The encoding of these bits is as follows:

Bit 1	Bit Ø	Word Length
Ø	Ø	5 Bits
Ø	1	6 Bits
1	Ø	7 Bits
1	1	8 Bits

Bit 2 specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is logic 1 when a 5-bit word length is selected with bits 0 and 1, 1-1/2 stop bits are generated or checked. If bit 2 is logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 stop bits are generated or checked.

Bit 3 is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed.)

Bit 4 is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic Ø, an odd number of logic 1's is transmitted or checked in the data word and parity bits. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5 is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and then detected by the receiver as a logic Ø if bit 4 is a logic 1, or it is transmitted and then detected as a logic 1 if bit 4 is a logic Ø.

Bit 6 is the Set Break Control bit. When it is a logic 1, the Serial OUTput (SOUT) is forced to the spacing state (logic Ø) and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic Ø. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7 is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the divisor latches (see below) or the Baud-Rate Generator during a read or write operation. It must be set low (logic Ø) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud-Rate Generator

The programmable Baud-Rate Generator is capable of taking the clock input (1.8432 MHz) and dividing it by any divisor from 1 to (2^{16}-1). The output frequency of the baud generator is 16 times the baud rate.

Divisor # = (frequency input)/(baud rate x 16)

Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to ensure the desired operation of the Baud-Rate Generator. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load.

Table 3-11 illustrates the use of the Baud-Rate Generator with a frequency of 1.8432 MHz. For baud rates of 9600 and below, the error obtained is minimal.

NOTE

The maximum operating frequency of the baud generator is 3.1 MHz. In no case should the data rate be greater than 9600 baud.

Table 3-11
BAUD RATE AT 1.843MHz

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16x CLOCK		% ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
	DECIMAL	HEX	
50	2304	900	—
75	1536	600	—
110	1047	417	0.026
134.5	857	359	0.058
150	768	300	—
300	384	180	—
600	192	0C0	—
1200	96	060	—
1800	64	040	—
2000	58	03A	0.69
2400	48	030	—
3600	32	020	—
4800	24	018	—
7200	16	010	—
9600	12	00C	—

FLOPPY DISK DRIVE

One or two floppy disk drives can be contained in the system unit. In the desktop unit, one drive can be replaced by a hard disk with a 10-megabyte capacity. Alternatively, a hard disk drive can be external to the system unit. A hard disk must be external to the Portable PC since half-size disk drives are used.

The Floppy Disk Drive (FDD) is double-sided, double-density with 40 tracks each side. It uses Modified Frequency Modulation (MFM) to read and write digital data. A series of sensor systems in the disk drive ensure the correct positioning and operation of the read-write head.

The floppy disk interface is integral to the PC board, and controls up to two disk drives that are mounted in the system unit. The interface is designed for double-density MFM-coded drives, and uses write precompensation logic with an analog phase-lock loop for clock and data recovery.

The drive motors, drive selection, and feature enable are controlled by the Digital Output Register (DOR). This is an output-only register. It is cleared by the I/O interface RESET line. Table 3-12 gives the bit definitions for the DOR.

Table 3-12
FLOPPY DISK CONTROLLER DIGITAL OUTPUT REGISTER (3F2 Hex)

BIT NO.	FUNCTION
0	If the drive motor is on: 0 selects drive A, 1 selects drive B
1	Spare
2	Enables FDC when set by program. Holds in reset when bit is 0
3	FDC interrupt and DMA request gated onto the I/O interface. Interrupt and DMA request I/O drivers disabled when bit is 0
4,5	Control the motors for drives A and B. If the bit is clear, the motor is off and the drive cannot be selected.
6,7	Spare

The Floppy Disk Controller (FDC) has two registers accessible to the CPU, a status register and a data register. The 8-bit status register can be accessed at any time. In actuality it is a stack of registers presented to the data bus one at a time. The status register also stores data, commands, and parameters. Data bytes are read from or written to the data register. Table 3-13 defines each bit in the main status register.

Table 3-13
MAIN STATUS REGISTER (3F4 Hex)

BIT NO.	SYMBOL	NAME	DESCRIPTION
DBØ	DAB	FDD A busy	Disk drive A is in seek mode
DB1	DBB	FDD B busy	Disk drive B is in seek mode
DB2	DCB		Spare
DB3	DDB		Spare
DB4	CB	FDC busy	READ or WRITE in progress
DB5	NDM	Non-DMA mode	Disk controller is in non-DMA mode
DB6	DIO	Data I/O	DIO = 1 data transfer from FDC data register to processor DIO = Ø data transfer from processor to FDC data register
DB7	RQM	Request Master	Bits DIO and RQM perform handshaking functions ready/direction with processor RQM indicates data register is ready to send/receive processor data

A number of data registers store data, commands, parameters, and provide floppy disk status information. Only one register is presented to the data bus at a time. There are fifteen commands for the Floppy Disk Controller. The multi-byte interchange of information between the processor and Floppy Disk Controller is a three-step operation: command, execution, and result.

Tables 3-14 to 3-17 provide bit definitions for command status registers Ø-3.

Table 3-14
COMMAND STATUS REGISTER Ø

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
D7 D6	Interrupt Code	IC	D7 = Ø, D6 = Ø Normal Termination (NT) of command. Command was properly executed. D7 = Ø, D6 = 1 Abnormal Termination (AT) of command. Execution of command was started but not successfully completed. D7 = 1, D6 = Ø Invalid command (IC) issue. A command that was issued was never started. D7 = 1, D6 = 1 Abnormal termination because ready signal from FDD changed state during command execution.
D5	Seek End	SE	When the FDC completes the seek command, this flag is set high (1).
D4	Equipment Check	EC	This flag is set if a fault signal is received from the FDD or if the track Ø signal fails to occur after 77 step pulses (recalibrate command).
D3	Not Ready	NR	This flag is set when the FDD is in the not-ready state and a read or write command is issued, or if a read or write command is issued to side 1 of a single-sided disk drive.
D2	Head Address	HD	This flag is used to indicate the state of the head interrupt.
D1 DØ	Unit Select 1 Unit Select 2	US1 US2	These flags are used to indicate a drive unit number at interrupt.

Table 3-15
COMMAND STATUS REGISTER 1

NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	End of Cylinder	EN	This flag is set when the FDC tries to access a sector beyond the final sector of the cylinder.
D6	—	—	Not used. This bit is always low (Ø).
D5	Data Error	DE	This flag is set when the FDC detects a Cyclic Redundancy Check (CRC) error in either the ID field or the data field.
D4	Over Run	OR	This flag is set if the FDC is not serviced by the main system during data transfers within a certain time interval.
D3	—	—	Not used. This bit is always low (Ø).
D2	No Data	ND	This flag is set during execution of a read data, write deleted data, or scan command, if the FDC cannot find the sector specified in the ID register. The flag is set during execution of the read ID command if the FDC cannot read the ID field without error. The flag is set during execution of a read cylinder command if the starting sector cannot be found.
D1	Not Writable	NW	This flag is set during execution of a write data, write deleted data, or format cylinder command if the FDC detects a write-protect signal from the FDD.
DØ	Missing Address Mark	MA	If the FDC cannot detect the ID address mark, this flag is set. At the same time, the MD (missing address mark in the data field) of status register 2 is set.

Table 3-16
COMMAND STATUS REGISTER 2

NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	—	—	Not used. This bit is always low (Ø).
D6	Control Mark	CM	This flag is set if the FDC encounters a sector that contains a deleted data address during execution of the read data or scan command.
D5	Data Error in Data Field	DD	This flag is set if the FDC detects a Cyclic Redundancy Check (CRC) error in the data.
D4	Wrong Cylinder	WC	This flag is set when the contents of C (the track number read from the disk) are different from those stored in the ID register. This bit is related to the ND bit (see Table 3-15).
D3	Scan Equal Hit	SH	This flag is set if the condition of "equal" is satisfied during execution of the scan command.
D2	Scan Not Satisfied	SN	This flag is set if the FDC cannot find a sector on the cylinder during execution of the scan command.
D1	Bad Cylinder	BC	This flag is set when the contents of C on the medium are different from those stored in the ID register, or when the content of C is FF. This bit is related to the ND bit.
DØ	Missing Address Mark in Data Field	MD	This flag is set if the FDC cannot find a data address mark or deleted data address mark when the data is read from the medium.

Table 3-17
COMMAND STATUS REGISTER 3

NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	Fault	FT	This bit is the status of the fault signal from the FDD.
D6	Write Protected	WP	This bit is the status of the write-protected signal from the FDD.
D5	Ready	RY	This bit is the status of the ready signal from the FDD.
D4	Track Ø	TØ	This bit is the status of the track Ø signal from the FDD.
D3	Two Side	TS	This bit is the status of the side select signal from the FDD.
D2	Head Address	HD	This bit is the status of the head address signal from the FDD.
D1	Unit Select 1	US1	This bit is the status of the unit-select-1 signal from the FDD.
DØ	Unit Select Ø	USØ	This bit is the status of the unit-select-Ø signal from the FDD.

PERSONAL HARD DISK DRIVE

The hard disk drive is a precision-engineered device that uses "Winchester" technology. The read/write heads are positioned 20 millionths of an inch above the rotating disk surface. The disk is in a sealed enclosure cooled by filtered air. It permits the storage of 10 Megabytes of data.

Accessible Registers

The Disk Controller Module (DCM) decodes read ports RDØ through RD3 and write ports WRØ through WR3. RD1 is not used.

The read port is activated by the $\overline{IOR}$ signal, the write port by the $\overline{IOW}$ signal.

Port 300 WRITE

A WRITE command to port 0300H (Fig. 3-13) will latch the data bus into a holding register to achieve the following:

Select drive Ø

Select head Ø through 7

Alter the step pulse level

Set the step direction

Select low write current

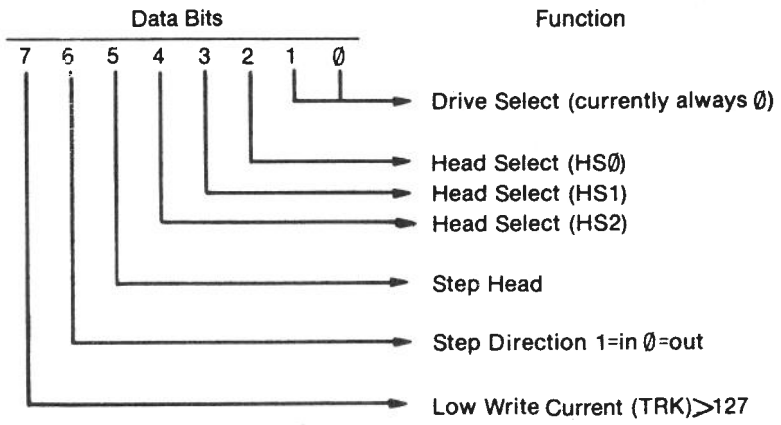


Fig. 3-13. I/O port address Ø3ØØH WRITE

Port 3Ø1 WRITE

A write command to port Ø3Ø1H (Fig. 3-14) will latch the data bus into a different register to achieve the following:

Select a sector

Select a disk READ or WRITE operation

Select ECC to be enabled

Select Write Precompensation

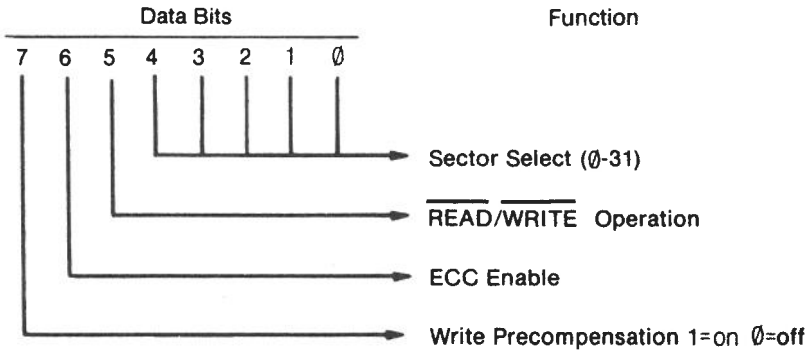


Fig. 3-14. I/O port address Ø3Ø1H WRITE

Port 3Ø2 WRITE

A write command to DCM port Ø3Ø2H enables Column Select ($\overline{CS}$) on the Random Access Memory.

Port 303 WRITE

A write command to DCM port 0303H initiates automatic write of 1 sector.

Port 300 READ

DCM port 300 (Fig. 3-15) provides status information including:

Drive type
Drive ready
Head-to-Track 0 position
Write fault from the disk drive
Seek complete
Loss of sync

A read command to port 0300H enables the controller to present DB2 and DB3 to be read by the system data bus.

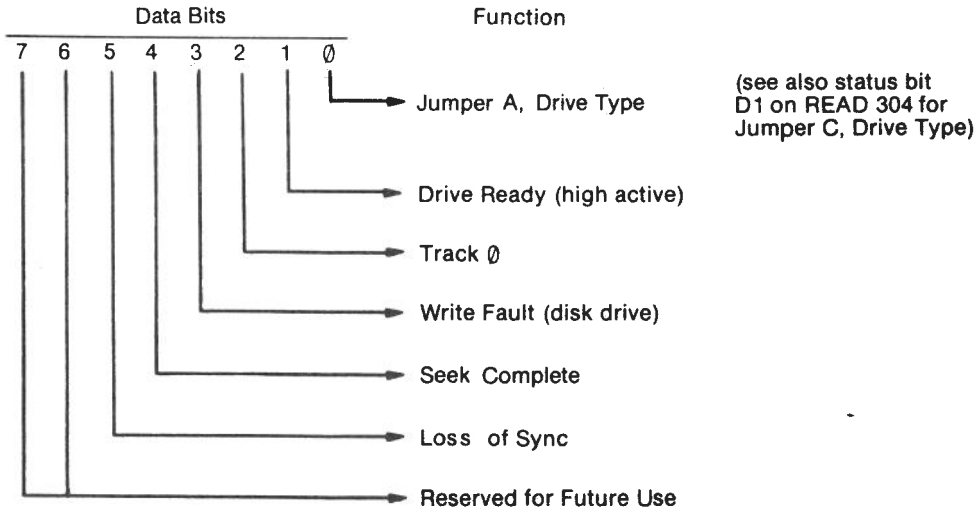

Data Bits
Function
7 6 5 4 3 2 1 0
Jumper A, Drive Type
(see also status bit D1 on READ 304 for Jumper C, Drive Type)
Drive Ready (high active)
Track 0
Write Fault (disk drive)
Seek Complete
Loss of Sync
Reserved for Future Use

Fig. 3-15. I/O port address 0300H READ

Port 301 READ

This port has no READ function.

Port 302 READ

DCM port 0302H READ being active enables transfer of data from DCM memory to system memory.

Port 303 READ

DCM READ port 0303H being active has the function of resetting memory address counter to a zero address state and resetting the ECC circuitry.

Ports 304-307 READ

DCM port 0304H - 0307H READ provides information on the type of drive in use, and a DCM busy status as shown in Fig. 3-16.

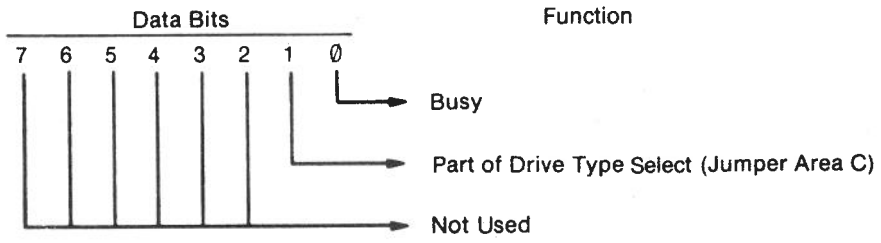


Fig. 3-16. I/O port address 0304H through 0307H READ

TIMING FUNCTIONS

The output of the 8255A-5 timer is programmable for a variety of system functions. Key timing functions and frequencies have been discussed in relation to the various logic and I/O functions.

The timer function also generates tones for the system speaker. Figure 3-17 shows how channel 2 and a gated clock input generate the output signal to the two-pin speaker connector.

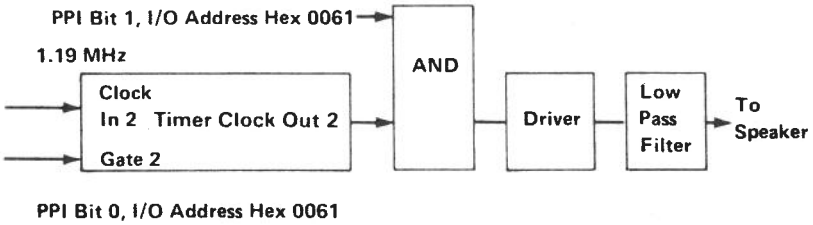


Fig. 3-17. Speaker driver system

REGISTERS FOR PROGRAMMABLE PERIPHERAL INTERFACE

The ports of the 8255-5 PPI are set by the program. Port A bits are programmed as inputs, port B bits as outputs. Port C has inputs and outputs. Table 3-18 shows the bit map for the 8255-5 ports.

Table 3-18
8255-5 I/O BIT MAP

PORT NUMBER (Hex)	I/O	PORT	FUNCTION
0060	Input	PA0	Keyboard Scan Code
		1	
		2	
		3	
		4	
		5	
		6	
		7	
0061	Output	PB0	+ Timer 2 gate speaker
		1	+ Speaker data
		2	Spare
		3	Spare
		4	Spare
		5	Spare
		6	- Hold keyboard clock low
		7	- Enable keyboard + Clear keyboard and enable sense switches
0062	Input	PC0	Ground
		1	+ 5 volts
		2	+ Planar RAM size 0
		3	+ Planar RAM size 1
		4	Ground
		5	+ Timer channel 2 Out
		6	Ground
		7	Ground
0063			Command/Mode Register

	7	6	5	4	3	2	1	0
Value	1	0	0	1	1	0	0	1

Hex 99

I/O EXPANSION SLOTS

Interface logic for the serial and parallel ports, floppy disk drives, and monitor are integrated with the PC system board. Four expansion slots extend the system capabilities. The I/O channel is fully compatible with any expansion board designed for the IBM PC.

Expansion boards use the I/O channel to gain access to the 8088 microprocessor bus. A 62-pin connector (Fig. 3-18) provides 20 address lines, an 8-bit bidirectional data bus, six levels of interrupt, three channels of direct memory access with control lines for I/O and memory read or write, and connections to clock and timing circuits. Associated control lines are provided. Power includes +5 vdc, +12 vdc, -12 vdc, and ground.

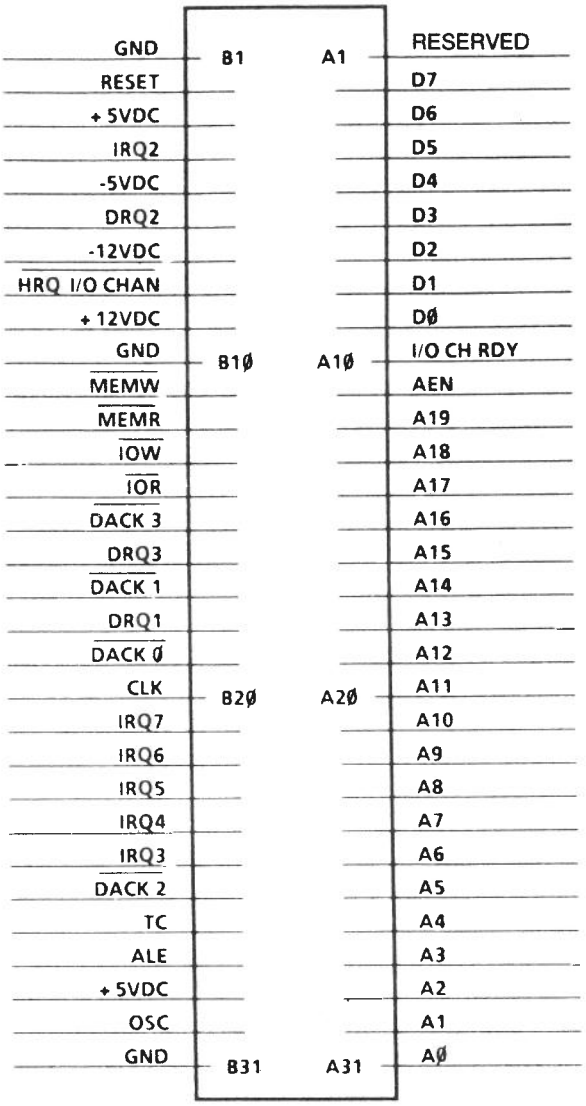


Fig. 3-18. I/O expansion slot and signals

Up to 65,536 I/O device addresses can be accessed through the I/O address map. Slow I/O and memory devices are buffered, and signal flow is controlled by a "ready" line activated by the device. If the ready line is not activated:

- Processor memory read and write cycles require 4 clocks (840 ns/byte)
- Processor I/O read and write cycles require 5 clocks (1.05 μs/byte)
- Refresh cycles occur every 72 clocks and require 4 clocks

Error conditions reported by the I/O channel check line, and parity errors in memory expansion cards activate a NonMaskable Interrupt (NMI) to the 8088 processor.

Table 3-19 describes the functions of each I/O channel signal.

Table 3-19
DESCRIPTION OF I/O CHANNEL SIGNALS

SIGNAL	I/O	DESCRIPTION
A0 - A19	O	These lines address I/O devices within the system and up to one megabyte of memory. A0 is the least significant bit (LSB) and A19 the most significant bit (MSB). These lines are active high, with signals from the processor or DMA controller.
D0 - D7	I/O	These lines are active high, and provide data bus bits for processor, memory, and I/O devices. D0 is the least significant bit (LSB) and D9 is the most significant bit (MSB).
ALE	O	The Address Latch Enable line from the 8288 bus controller is used to latch valid addresses from the processor. The trailing edge of ALE latches the address on the system board. It confirms for the I/O channel that the processor address is valid.
OSC	O	The 14.31818 MHz OSCillator, with a 50% duty cycle, is the system time base.
CLK	O	The system clock divides the oscillator frequency by three (4.77 MHz) and has a period of 210 ns.
I/O CH RDY	I	This line signifies I/O CHannel ReaDY when high, not ready when low. It is normally high and pulled low by memory or I/O devices to interface slower devices to the system. The device should immediately drive the line low when a valid address and a read or write command is detected. The line should not be held low longer than ten clock cycles. I/O or memory cycles are extended by an integral number of 210 ns clock cycles.
$\overline{\text{I/O CH CK}}$	I	This I/O CHannel ChecKs and communicates parity or error information on I/O channel memory or devices. A parity error is indicated by an active low signal.

Table 3-19
DESCRIPTION OF I/O CHANNEL SIGNALS (Concluded)

SIGNAL	I/O	DESCRIPTION
IRQ2 - IRQ7	I	These Interrupt ReQuest lines signal the processor that an I/O device requires attention. IRQ2 has the highest priority and IRQ7 the lowest. A high signal initiates an interrupt request. It is held high until acknowledged by the processor.
$\overline{\text{IOR}}$	O	A Read command to an I/O device initiates transfer of data to the data bus. The signal is active low, and may be driven by the processor or DMA controller.
$\overline{\text{IOW}}$	O	A Write command instructs an I/O device to read data from the data bus. The signal is active low, and may be driven by the processor or DMA controller.
$\overline{\text{MEMR}}$	O	The MEMory Read command instructs the memory to send data to the data bus. The signal is active low, driven by the processor or DMA controller.
$\overline{\text{MEMW}}$	O	The MEMory Write command line instructs the memory to store the data that is on the data bus. The signal is active low, driven by the processor or DMA controller.
DRQ1-DRQ3	I	The DMA ReQuest lines are asynchronous channels used by peripheral devices that require DMA service. DRQ1 has the highest priority and DRQ3 the lowest. An active high line initiates a request, and the DRQ line is held high until the corresponding DACK line becomes active.
$\overline{\text{DACK0}}$ - $\overline{\text{DACK3}}$	O	These lines ACKnowledge DMA requests from DRQ1-DRQ3. $\overline{\text{DACK0}}$ is used to refresh system dynamic memory. DACK lines are active low.
AEN	O	The Address ENable line precludes use of the I/O channel by the processor and other devices while DMA transfers take place. When the line is active high, the DMA controller directs the activity of the address bus, data bus, I/O and memory read command lines, and I/O and memory write command lines.
TC	O	The Terminal Count line provides an active high signal when the terminal count is reached for any DMA channel.
$\overline{\text{HRQ I/O CH}}$		The Hold ReQuest line for the I/O CHannel is used by peripheral devices to halt the processor. The active low signal is sent to the bus arbitrator.

MEMORY UTILIZATION

The 8088 central processing unit can address 1024K bytes (100000 H) of memory. Table 3-20 is a system memory map showing the optional and reserved areas of memory.

Table 3-20
SYSTEM MEMORY MAP

START ADDRESS DECIMAL	START ADDRESS HEX	FUNCTION
0	00000	**System Memory on PCB**
64K	10000	128K Dynamic Memory
128K	20000	
192K	30000	128K Memory (optional)
256K	40000	
320K	50000	128K Memory (optional)
384K	60000	
448K	70000	128K Memory (optional)
512K	80000	
576K	90000	128K I/O Channel RAM Space
640K	A0000	
704K	B0000	**128K Reserved** Alphanumeric Screen 4K at B0000 Color/Graphics 16K at B8000
768K	C0000	
832K	D0000	Hard Disk Control at C8000
896K	E0000	**Reserved for 192K ROM**
960K	F0000	ROM BIOS 8K at FE000
1024K	FFFFF	

Note: PC monochrome graphics require 32K per graphic page, and pages 0 through 7 start at 00000H in the default mode. Starting address can be moved to 40000H using an internal jumper on the main PC board.

There is provison for four blocks of 128K on the main PC board starting at decimal 0 (00000H). A ROM BIOS routine determines the amount of system memory during initialization. Blocks smaller than 128K cannot be used on the system board.

The ROM BIOS (Section 5) does not determine the memory available on expansion boards unless there is 512K of memory on the main PC board. I/O channel RAM space starts at 512K (80000H) and extends to 704K (B0000), the start address for screen memory. Memory addresses above this level are reserved for color graphics, hard disk, and the BIOS, as shown in Table 3-20. Because memory addresses less than 512K (80000H) are allocated to system dynamic RAM, these cannot be used by expansion boards, even if there is less than 512K of memory on the system board.

The ROM BIOS does not look for controller boards. Therefore memory start addresses must be entered from the program. The CONFIG command in DOS can be used to turn on the DMA memory refresh, if an expansion board requires it. Normally, any expansion board which has memory will require DMA refresh.

Section 4
SUPER-RESOLUTION GRAPHICS

Super-resolution graphics are achieved using the same graphic matrix used for super-resolution characters. Twenty-five lines of characters thirteen pixels high gives a vertical resolution of:

25 X 13 = 325 lines

The graphics use half of the horizontal resolution of the alphanumeric characters, equivalent to eighty characters times eight pixels wide. The horizontal graphics resolution is thus:

80 X 8 = 640 pixels

The total number of individually addressable picture elements (pixels) on the super-resolution black and white graphics screen is:

325 X 640 = 208,000 pixels

MEMORY ADDRESS

Jumper Area B on the main PC board must be jumpered from pin 2 to pin 4 for graphics in the first 256K of memory. This is the default configuration. Jumpering pin 1 and pin 3 selects graphics in the second 256K. GWBASIC requires the graphics to be in the first 256K of memory.

GRAPHIC PAGES

The graphic screens reside in dynamic RAM in the main memory. Each screen occupies 26,000 bytes and may reside in any 32K boundary in memory. Up to 256K of memory can be allocated for graphics, permitting up to 8 graphic pages. The absolute addresses for pages 0-7 can be calculated using the formula:

ADDR = PAGE x 8000H

The specific page addresses starting at 00000H are as follows:

PAGE	SEGMENT	PAGE	SEGMENT
0	00000H	4	20000H
1	08000H	5	28000H
2	10000H	6	30000H
3	18000H	7	38000H

To manipulate the picture elements with PEEKs and POKEs using GWBASIC, set the data segment to the corresponding graphic page. For graphic page 7, DEFine the SEGment with DEF SEG as follows:

DEF SEG = &H38000

GRAPHIC MEMORY ORGANIZATION

The memory is arranged as 325 lines of 80 contiguous bytes. Each line requires:

80 bytes X 8 bits per byte = 640 bits

Each pixel is stored in a single bit, where 0 = black and 1 = white (or green). The least significant bit is displayed first, and the most significant bit last, as shown in Fig. 4-1.

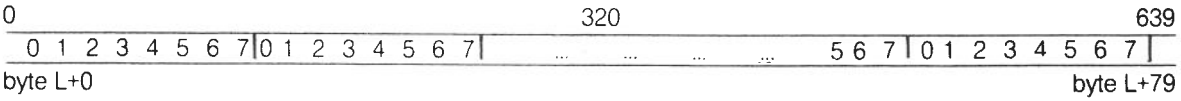


Fig. 4-1. 640 pixel line graphics screen

The address for any pixel on the screen can be addressed in terms of line number and position, as indicated in Table 4-1.

Table 4-1
MEMORY ADDRESSES FOR GRAPHIC SCREEN

LINE NO.	ADDRESS + OFFSET	BLOCK NO.	SUB-LINE
0	0 x 2048 + 0 x 80	0	0
1	1 x 2048 + 0 x 80		1
2	2 x 2048 + 0 x 80		2
... ...			
11	11 x 2048 + 0 x 80		11
12	12 x 2048 + 0 x 80		12
13	0 x 2048 + 1 x 80	1	0
14	1 x 2048 + 1 x 80		1
... ...			
24	11 x 2048 + 1 x 80		11
25	12 x 2048 + 1 x 80		12
312	0 x 2048 + 24 x 80	24	0
313	1 x 2048 + 24 x 80		1
... ...			
323	11 x 2048 + 24 x 80		11
324	12 x 2048 + 24 x 80		12

The 325 lines are grouped into 25 blocks of 13 lines. The address of any line can be calculated by taking the line within the block (Ø - 12) multiplied by 2Ø48, and summing with the block number (Ø - 24) multiplied by 8Ø.

PROGRAMMING WITH ASSEMBLY LANGUAGE

The formula for calculating an address and mask for the super-resolution monochrome graphics is as follows:

$$ADDRESS = (2048 \times (Y \text{ MOD } 13)) + (80 \times INT(Y/13)) + (INT\ (X/8))$$

$$MASK = 2^{(X \text{ MOD } 8)}$$

In the following algorithms, ES is the memory segment where the graphic screen resides, BX is the address of the pixel, and AL is the pixel mask. The address points to the byte containing the desired pixel, and the mask isolates the pixel within the byte.

Use the following code to set, erase, toggle, or test points:

Set a Point:

```
OR      ES: [BX], AL        ; Set bit in graphic screen
```

Erase a Point:

```
NOT     AL                  ; Reserve bit mask
AND     ES: [BX], AL        ; Mask off pixel
```

Toggle a Point:

```
XOR     ES: [BX], AL        ; Toggle pixel
```

Test a Point:

```
TEST    ES: [BX], AL
JNZ     Pixel Set           ; Point is on
...                         ; Point is off
```

The following machine language routine calculates an address and mask for setting or resetting a point. The X position should be passed in the CX register and the Y position in the DX register. The address is returned in the BX register and the mask in the AL register.

```
MAPXYC  PROC
        PUSH    CX
        PUSH    BP
        PUSH    ES
        MOV     AX,DRAWING_SEG      ;Memory segment where the
        MOV     ES,AX               ;graphics screen is located
        MOV     AX,DX
        MOV     BL,13
        DIV     BL
        MOV     BH,AL
        AND     BX,0FF00H
        ROR     BX,1
        ROR     BX,1
        MOV     BP,BX
        ROR     BP,1
        ROR     BP,1
        ADD     BX,BP
        AND     AX,0F00H
        ROL     AX,1
        ROL     AX,1
        ROL     AX,1
        ADD     BX,AX
        MOV     AX,CX
        SHR     AX,1
        SHR     AX,1
        SHR     AX,1
        ADD     BX,AX
        MOV     AL,128
        AND     CL,7
        INC     CL
        ROL     AL,CL
        POP     ES
        POP     BP
        POP     CX
        RET
MAPXYC  ENDP
```

The following routine sets the 6845 video controller chip to point to the graphics display segment addressed by DRAWING_SEG. For the cursor to remain on the screen, a cursor position routine must be written. The CURSOR_HIGH register (0EH) in this chip needs to point to the same segment of memory as in the START_HIGH register (0CH), which always points to the graphics screen. Refer to a 6845 data sheet for more information on programming this chip.

```
GRDISP   PROC
         MOV     DX,3B4H              ;DX = Address of 6845
         MOV     CX,DRAWING_SEG       ;CX = Graphics segment
         MOV     AH,CH                ;Graphics segment high
         MOV     AL,0CH               ;6845 register 0CH
         OUT     DX,AL                ;Select register 0CH
         MOV     AL,AH
         INC     DX
         OUT     DX,AL                ;Set register 0CH = Graphic segment high
         DEC     DX
         MOV     AL,AH                ;Graphics segment low
         MOV     AL,0DH               ;6845 register 0DH
         OUT     DX,AL                ;Select register 0DH
         MOV     AL,AH
         INC     DX
         OUT     DX,AL                ;Set register 0DH = Graphic segment low
         RET
GRDISP   ENDP
```

An alternative means to set the graphics page is as follows:

```
         MOV     DX,3B4H              ;CRT index port
         MOV     AL,12                ;CRT start address (high)
         OUT     DX,AL                ;Select CRT register
         INC     DX                   ;CRT data port
         MOV     AL,00ppp000B         ;ppp is graphics page 0 - 7
         OUT     DX,AL                ;Select graphics page
```

The following code will enable graphics only, text only, or mixed text and graphics:

Enable Graphics Only:

```
MOV     DX, 3B8H
MOV     AL, 0A0H
OUT     DX, AL
```

Enable Text Only:

```
MOV     DX, 3B8H
MOV     AL, 28H
OUT     DX, AL
```

Enable Graphics and Text:

```
MOV     DX, 3B8H
MOV     AL, 0A8H
OUT     DX, AL
```

NOTE

Table 3-5 in Section 3 is the port address map for port 3B8H.

Section 5
BASIC INPUT OUTPUT SYSTEM

Input/Output interfaces and peripheral I/O devices are controlled by the Basic Input Output System (BIOS) ROM on the main PC board. The BIOS facilitates program implementation by providing control of peripheral hardware. It also provides routines for assembly language programmers. The BIOS ROM performs a variety of operations without concern for the address or operating characteristics of the device.

The DOS and BIOS are designed to be compatible with programs designed to operate on PC DOS, and use the same entry points. For this reason, assembly language programs must be developed using the IBM assembler. "Internal errors" will be generated if the Microsoft assembler is used.

Specific programming information for the BIOS ROM is presented in Appendix D. In general, programming is consistent with the procedures outlined in the IBM Personal Computer MACRO Assembler Manual and the BIOS listings in Appendix A of the IBM Technical Reference Manual.

PARAMETERS AND VECTORS

8088 software interrupts give access to the BIOS, and all parameters passed to and from BIOS routines must go through the 8088 registers.

Table 5-1 lists the software interrupts for the 8088 CPU. Table 5-2 lists the 8088 hardware interrupts.

READ/WRITE MEMORY USAGE

Parameters for BIOS routines go through 8088 registers. The prologue for each BIOS function indicates the registers used for the call and return. The AH register is used to specify the function where more than one operation is possible. BIOS routines save all registers except for AX and flags. The prologue to the BIOS function shows exact register usage.

BIOS routines use 256 bytes of memory starting at absolute Hex 400. During power-on initialization and bootstrap, memory locations 300 to 3FF are used as a stack area, unless otherwise set up by the user.

Table 5-3 shows the GWBASIC and DOS reserved interrupts. Table 5-4 shows reserved memory locations.

Programmers should not use fixed addresses for BIOS codes in applications programs because these addresses are subject to change. Also, when altering I/O bit codes, it is advisable to change only those bits essential for the current task, and immediately restore them to the initial values to avoid program errors.

Table 5-1
8088 SOFTWARE INTERRUPTS

INTERRUPT NO.	HEX ADDRESS	FUNCTION	BIOS ENTRY
0	0-3	Divide by zero	D11
1	4-7	Single step	D11
2	8-B	Nonmaskable	NMI_INT
3	C-F	Breakpoint	D11
4	10-13	Overflow	D11
5	14-17	Print screen	PRINT_SCREEN
6	18-1B	Reserved	D11
7	1D-1F	Reserved	D11
8	20-23	Time of day	TIMER_INT
9	24-27	Keyboard	KB_INT
A	28-2B	Reserved	D11
B	2C-2F	Communications	D11
C	30-33	Communications	D11
D	34-37	Disk	D11
E	38-3B	Diskette	DISK_INT
F	3C-3F	Printer	D11
10	40-43	Video	VIDEO_IO
11	44-47	Equipment Check	EQUIPMENT
12	48-4B	Memory	MEMORY_SIZE_DETERMINE
13	4C-4F	Diskette/disk	DISKETTE_IO
14	50-53	Communications	RS232_IO
15	54-57	Cassette	(unused)
16	58-5B	Keyboard	KEYBOARD_IO
17	5C-5F	Printer	PRINTER_IO
18	60-63	Resident BASIC	(unused)
19	64-67	Bootstrap	BOOT_STRAP
1A	68-6B	Time of day	TIME_OF_DAY
1B	6C-6F	Keyboard break	DUMMY_RETURN
1C	70-73	Timer tick	DUMMY_RETURN
1D	74-77	Video initialization	VIDEO_PARMS
1E	78-7B	Diskette parameters	DISK_BASE
1F	7C-7F	Graphic/character video	0

Table 5-2
8088 HARDWARE INTERRUPTS

NUMBER	APPLICATION
NMI	Parity
1	Timer
2	Keyboard
3	Secondary asynchronous communications and synchronous (SDLC) communications
4	Primary asynchronous communications and synchronous (SDLC) communications
5	Hard disk
6	Diskette
7	Parallel printer

Table 5-3
GWBASIC AND DOS INTERRUPTS

INTERRUPT	ADDRESS	FUNCTION
20	80-83	DOS program terminate
21	84-87	DOS function request
22	88-8B	DOS terminate address
23	8C-8F	DOS Ctrl Break exit address
24	90-93	DOS fatal error vector
25	94-97	DOS absolute disk read
26	98-9B	DOS absolute disk write
27	9C-9F	DOS terminate, fix in storage
28-3F	A0-FF	Reserved for DOS
40-5F	100-17F	Reserved
60-67	180-19F	Reserved for user software interrupts
68-7F	1A0-1FF	Not used
80-85	200-217	Reserved for GWBASIC
86-F0	218-3C3	Used by GWBASIC interpreter
F1-FF	3C4-3FF	Not used

Table 5-4
RESERVED MEMORY LOCATIONS

MODE	HEX ADDRESS	FUNCTION
ROM BIOS	400-48F	See Appendix D - ROM BIOS Listing
	490-4EF	Reserved
	4F0-4FF	Reserved for programmer application
	500-5FF	Reserved for DOS and GWBASIC
DOS	500	Print-screen status flag store 0-Print-screen not active or successful print operation 1-Print-screen in progress 255-Error during print-screen operation
DOS	504	Single drive mode status byte
GWBASIC	510-511	Segment address storage for GWBASIC
GWBASIC	512-515	Clock interrupt vector segment: offset store
GWBASIC	516-519	Break key interrupt vector segment: offset store
GWBASIC	51A-51D	Disk error interrupt vector segment: offset store

EXPANSION BOARDS AND SYSTEM ACCESSIBLE ROM MODULES

The BIOS ROM facilitates integration of I/O expansion boards during system initialization. Default vectors are first established, and the system is scanned for additional ROM modules. At this time, ROM routines on the expansion boards establish or intercept interrupt vectors, and the I/O function is integrated with the system.

Absolute addresses hex C8000 through F4000 are scanned in 2K blocks for valid ROM addresses. A valid ROM will return the following values:

Byte 0	hex 55
Byte 1	hex AA
Byte 2	number of 512 byte blocks in ROM (validated by CHECKSUM)

When the ROM is found to be valid, there is a call to byte 3 of the ROM, which enables the expansion board to perform power-on initialization. Control is then returned to the BIOS.

KEYBOARD FUNCTIONS AND CODES

The BIOS extends the ASCII code to encompass values from Ø to 255 using the Ctrl and Alt keys. The BIOS suppresses some key combinations. Appendix E lists the control codes, characters and functions generated with the typewriter, special, and function keys, and the functions generated with the numeric keypad/arrow keys.

Altered shift states result when the following keys are used:

Shift	Upper case or numbers on numeric keypad
Ctrl	Programming codes and special functions
Alt	Alternate character/graphic/symbol/function
Scroll Lock	Screen or cursor control or break
Caps Lock	Upper case for alpha keys only

Combinations of Alt, Ctrl, and Shift are not valid, except for Alt-Ctrl in the system reset function. When two or more of these keys are pressed at the same time, only one is valid. The order of precedence is Alt, Ctrl, and Shift.

DOS SPECIAL KEY FUNCTIONS

Table 5-5 lists special key functions for the Disk Operating System (DOS).

Table 5-5
DOS SPECIAL KEY FUNCTIONS

KEY OR KEYS	FUNCTION
Ctrl Num-Lock	Stop processing
Ctrl PrtSc	Turn on echo to printer
Ctrl N	Stop printer echo
Ctrl Break	Stop current function
Ctrl H	Backspace
Ctrl J	Line feed
Ctrl X	Cancel line
→	Copy character
F2	Copy from margin to specified character
F3	Copy remaining characters
Del	Skip character
F4	Skip characters until match
F1Ø	Exit insert mode
Ins	Enter insert mode
F5	Write the line to the template

I/O PORT ADDRESS MAP

Table 5-6 provides an address map for I/O ports to access DMA registers and functions, Programmable Interrupt Controller, Programmable Interval Timer, Programmable Peripheral Interface, and NonMaskable Interrupt registers. Ports for the integral I/O interfaces and expansion boards are also listed.

Table 5-6
PORT ADDRESS MAP

HEX RANGE	ADDRESS BIT 9	8	7	6	5	4	3	2	1	0	DEVICE
00-0F	0	0	0	0	0	*	A3	A2	A1	A0	DMA Chip 8237A
20-21	0	0	0	0	1	*	*	*	*	A0	Interrupt 8259A
40-43	0	0	0	1	0	*	*	*	A1	A0	Timer 8253-5
60-63	0	0	0	1	1	*	*	*	A1	A0	PPI 8255-5
80-83	0	0	1	0	0	*	*	*	A1	A0	DMA Page Registers
AX**	0	0	1	0	1						NMI Mask Registers
CX	0	0	1	1	0						Reserved
EX	0	0	1	1	1						Reserved
200-20F	1	0	0	0	0	0	A1	A2	A1	A0	Game I/O Adapter
278-27F	1	0	0	1	1	1	1	*	A1	A0	Reserved
2F8-2FF	1	0	1	1	1	1	1	A2	A1	A0	Reserved
300-307	1	1	0	0	0	0	0	A2	A1	A0	Hard Disk I/O Ports
378-37F	1	1	0	1	1	1	1	*	A1	A0	Auxiliary Parallel Printer Port
3B0-3BF	1	1	1	0	1	1	A3	A2	A1	A0	Built-in Parallel Printer Port and Monochrome Display
3D0-3DF	1	1	1	1	0	1	A3	A2	A1	A0	Color/Graphics Adapter
3F0-3F7	1	1	1	1	1	1	0	A2	A1	A0	5 1/4" Drive
3F8-3FF	1	1	1	1	1	1	1	A2	A1	A0	TP RS-232C CD (Serial Port)

* Not in decode

** NonMaskable Interrupt (NMI) to the 8088 is disabled by external hardware at power-on. This can be set and reset as follows:

To set mask: Write 80H to I/O Address 0A0H
To clear mask: Write 000 to I/O Address 0A0H

Appendix A
PC PUBLICATIONS AND SUGGESTED REFERENCES

PC User's Guide, P/N 700061
Shipped with each computer.
Target audience: end user.

DOS Manual, P/N 700004
Shipped with each computer.
Target audience: end user.

MultiMate Manual, P/N 700028
Shipped with each computer.
Target audience: end user.

GWBASIC Manual, P/N 700023
Shipped with each computer.
Target audience: end user.

Corona PC Service Manual, P/N 700029, $50.
Covers Installation Procedure, Principles of Operation, Troubleshooting to a Subassembly Level, Adjustments, and Removal/Replacement Procedures.
Target audience: Service technician performing subassembly troubleshooting.

Corona PC Training Manual, P/N 700030
Provides a self-administered training course for subassembly troubleshooting.
Target audience: Service technician performing subassembly troubleshooting.

Corona PC Technical Manual, P/N 700031, $130.
Covers Installation Procedures, System Troubleshooting, Adjustments, Removal/Replacement, Main PCB Theory of Operation, Main PCB Troubleshooting to the Component level. All information contained in the Service Manual is also in the Technical Manual.
Target audience: Service technician performing component level troubleshooting.

MPI Model 51/52 Floppy Disk Produce Manual, P/N 700046, $50.
Covers Installation and Checkout, Theory of Operation, Maintenance, and Troubleshooting.
Target audience: Service technician performing adjustments and troubleshooting on the MPI Floppy Drives.

Seagate ST 406/412/419 OEM Manual, P/N 700047, $10.
Covers Functional Characteristics, Functional Operations, Electrical and Physical Interface, Physical Specifications, and Track Format.
Target audience: People interested in the product specifications of the Winchester Drive.

Seagate ST 406/412 Maintenance Manual, P/N 700048, $10.

Covers Theory of Operation, Maintenance, and Repair.
Target Audience: Service technicians performing adjustments and troubleshooting.

Corona EPHD Service Manual, P/N 700050, $30.

Covers Theory of Operation, Removal and Replacement, and Adjustments of the External Personal Hard Disk.
Target audience: Service technicians performing adjustments and troubleshooting.

Corona IPHD Service Manual, P/N 700051, $30

Covers Theory of Operation, Removal and Replacement, and Adjustments of the Internal Personal Hard Disk.
Target audience: Service technicians performing adjustments and troubleshooting.

Appendix C
GLOSSARY OF SIGNAL NAMES

NOTE:

These signal names relate to the main PC board. Signals which relate to disk and communication ports can be found in Section 2 and Section 3. Signals are listed in the states that most often apply. Signals may be inverted before they are used.

ADSTB — Address Strobe. This signal is used by the DMA Controller to latch Address lines A8-A15, which are multiplexed with DMA Data lines DØ-D7.

AEN — Address Enable. This is an active high signal that is generated by inverting the (active low) AEN BD signal. It recludes the use of the I/O channel by the processor and other devices while DMA transfers take place. When the line is active high, the DMA Controller directs the activity of the address bus, data bus, I/O and memory read command lines, and I/O and memory write command lines. AEN is used in several areas of the computer for address latching.

$\overline{\text{AEN BD}}$ — Address Enable--BD. This signal is generated by the Bus Arbitrator. It is used to "float" the data and address buffers connected to the CPU when the system buses are taken over by the DMAC or by a device connected to an expansion slot. It also goes to the Register File used in DMA page number selection. This signal is used in its active low and active high states.

ALE — Address Latch Enable. This signal is produced by the 8288 Bus Controller. This signal is active high, and is used to latch valid addresses from the processor. The trailing edge of ALE latches the address on the system board. It confirms for the I/O channel that the processor address is valid. It is also sent to the expansion slots, where it is used to latch addresses at the proper times for correct system operation.

AMUX — Address Multiplex. The AMUX signal is active high. It is produced by the memory row and column select logic to multiplex system memory addresses.

AØ-A19 — These lines address I/O devices within the system and up to one megabyte of memory. AØ is the least significant bit (LSB) and A19 the most significant bit (MSB). These lines are active high, with signals from the processor or DMA Controller.

$\overline{\text{CAS}}$Ø-$\overline{\text{CAS7}}$ — Column Address Select. These active low signals are used to access the columns of cells in the system memory. With the RAS signals, these allow the CPU or Video Controller to access any individual cell in the RAM. The CAS signals are produced in the memory row and column select logic, and go to the system memory.

Glossary of Signal Names

CLK	System Clock. This is the master clock for the 8088 CPU. It is produced by the clock generator by dividing the oscillator frequency (14.31818 MHz) by three to produce a clock (CLK) frequency of 4.77 MHz. It has a period of 210 ns.
CLK	Keyboard Clock. This clock signal is used for timing the microcomputer chip in the keyboard unit and the keyboard interface on the main PCB. This signal is generated under the control of port "B" of the Programmable Peripheral Interface.
CLK	Floppy Disk Controller Clock. This is an 8-MHz square wave signal used for overall timing by the floppy disk controller.
$\overline{\text{CRT CONT}}$	CRT Control. This is an active low signal produced by the address decoder. It is sent to the video process logic to enable the video display.
$\overline{\text{CRT STATUS}}$	CRT Status. This address decoder signal is active low. It is sent through the light pen logic to the port through which the CPU reads information about light pen status and position.
CURSOR	Cursor. Video controller generates this signal and sends it to the video process logic to produce the cursor on the monitor screen.
C/$\overline{V}$, $\overline{C}$/V	CPU/Video Controller. This signal is produced by the video timing logic. The two inverse forms of this signal are used to enable or disable multiplexers which allow the video controller or the CPU to address the system memory.
$\overline{\text{DACK0}}$-$\overline{\text{DACK3}}$	DMA Acknowledge. These active low signals are sent out by the Direct Memory Access Controller (DMAC) in response to Data ReQuest (DRQ) signals. These tell the peripherals or components requesting a DMA transfer that the request has been received. $\overline{\text{DACK0}}$ is used to refresh system dynamic memory.
DATA	Keyboard Character Data. Coded serial information from the keyboard is sent to keyboard interface. Here it is changed into parallel ASCII data for transmission to the programmable peripheral interface, and then to the data bus.
DEN	Data Enable. This active high signal is generated by the bus controller and used by the transceiver to demultiplex data from the CPU bus onto the system data bus.
DIR	Head Direction. This signal is used to tell the read/write head in the disk drive unit to move inward or outward, depending on the state of the signal. After the direction has been determined, the STEP signal is used to tell the head how many steps to take. This signal is sent out by the FDC, through a multiplexer and gate.
DISPEN	Display Enable. The video controller generates this signal, which is provided to the video process logic to enable the display logic.
DMA CLK	DMA Clock. This clock, which is generated in the bus arbitrator circuitry, is the master clock for Direct Memory Access (DMA) timing. It operates at the same 4.77 MHz frequency as the main system clock (CLK) generated by the clock generator.

DMA RDY	DMA Ready. This active high signal is sent from the Wait-State Generator to the Direct Memory Access Controller (DMAC). It is used to synchronize the DMAC with slower memory and peripheral devices.
DRQØ-DRQ3	DMA Request. These lines are asynchronous channels used by peripheral devices which require DMA service. When the floppy disk controller or a device connected to one of the expansion slots requires a DMA transfer, it sends an active high DRQ signal to the DMAC. This request is acknowledged by a DACK signal. DRQØ has the highest priority, and DRQ3 the lowest. The DRQ line is held high until the corresponding DACK line becomes active.
DT/R	Data Transmit/Receive. This signal determines the direction in which data is transferred. If this signal is high, data is transmitted from the CPU to the system data bus for an I/O write operation. If it is low, data is received (read) by the CPU from the data bus.
DØ-D7	These lines are active high, and provide data bus bits for processor, memory, and I/O devices. DØ is the least significant bit (LSB) and D7 is the most significant bit (MSB).
$\overline{\text{EOP}}$	End of Process.This active low signal from the Direct Memory Access Controller (DMAC) is inverted to generate the Terminal Count (TC) signal.
HLDA	Hold Acknowledge. When the DMAC requests control of the system buses (by means of the HRQ DMA signal), the bus arbitrator sends back this acknowledgment. This tells the DMAC that it now has control of the buses, and the CPU is stopping to allow the transfer to occur. This signal is active high.
$\overline{\text{HRLD}}$	High-Resolution (Graphics) LoaD. This signal loads the graphic shift registers and is active low.
$\overline{\text{HRQ DMA}}$	Hold Request--DMA. This signal, from the Direct Memory Access Controller (DMAC) to the bus arbitrator, is used by the DMAC to request control of the system buses and to halt the processor at the appropriate times so that a DMA transfer can occur. This is an active low signal.
$\overline{\text{HRQ I/O CH}}$	Hold Request--Input/Output Channel. When a device connected to one of the expansion slots needs to halt the processor, this active low signal is sent to the bus arbitrator. It is similar to the $\overline{\text{HRQ DMA}}$ signal from the DMA controller.
HR VIDEO	High-Resolution Video. This signal has its origin in shift registers used for converting parallel high-resolution graphics information to serial form. The serial output of these shift registers is sent to the video process logic to produce high-resolution displays.
HSYNC	Horizontal Synchronization. The HSYNC signal is produced by the video controller and provided through inverters to the video connector.
$\overline{\text{INDEX}}$	Index. This signal is sent from the hard disk drive to the Phased-Lock Loop (PLL) circuit to provide a clock counter. Matching this with the frequency of outputs SØ' to S4' keeps the PLL circuit in lock.

$\overline{\text{INT}}$	Interrupt. When the Interrupt Controller receives a request for service, it sends this signal to the CPU to interrupt its operation. At the same time, it outputs an address to the address bus that tells the CPU where to find the routine for performing the service required. This is an active low signal.
$\overline{\text{INTA}}$	Interrupt Acknowledge. After receiving the INT signal from the Interrupt Controller, the CPU causes the Bus Controller to send this active low signal to the Interrupt Controller to confirm that the CPU has received its request for a service routine.
$\overline{\text{INDEX}}$	Index Hole Sensed. This active low signal is generated by a sensor in the floppy disk drive unit when the index hole is sensed. It provides a reference for the Floppy Disk Controller to use in determining where the first sector of each track begins.
$\overline{\text{INTR}}$ CS	Interrupt Controller Chip Select. This signal comes from the address decoder and enables the Interrupt Controller during system operation. This signal is active low.
I/O CH RDY	Input/Output Channel Ready. This is an active high signal that is used to synchronize devices connected to the expansion slots with memory or other devices that operate at a slower speed. The device should immediately drive the line low when a valid address and a read or write command is detected. The line should not be held low longer than ten clock cycles. I/O or memory cycles are extended by an integral number of 210 ns clock cycles.
$\overline{\text{I/O CH CK}}$	Input/Output Channel Check. This line checks and communicates parity or error information on I/O Channel memory or devices. A parity error is indicated by an active low signal.
$\overline{\text{IOR}}$	Input/Output Read. This control signal allows the CPU to read information from a register in an input/output device or PC board interface component. A read command initiates transfer of data to the data bus. The signal is active low, and may be driven by the processor or DMA controller.
$\overline{\text{IOW}}$	Input/Output Write. This control signal allows the CPU to write information into a register in an input/output device or PC board interface. It is an active low signal.
IRQ0-IRQ7	Interrupt Request. These signals are generated by certain components in the system when they need service from the 8088 CPU. They are sent to the Interrupt Controller which in turn sends an interrupt signal to the CPU. These active high signals are held high until acknowledged by the processor.
$\overline{\text{LOCK}}$	Lock. The lock signal from the CPU tells the Bus Controller and the Bus Arbitrator that the buses should not be given up. This prevents one master component from taking control of the buses away from another between bus cycles. This is an active low signal.
$\overline{\text{LP CLR}}$	Light Pen Clear. This active low signal is produced by the address decoder and used in the light pen logic (with the LPEN IN and LPEN SET signals) to produce the LPEN STB signal.

LPEN IN	Light Pen Input. This is the signal from the photo sensor in the light pen. It is used to produce the LPEN STB signal.
$\overline{\text{LPEN SET}}$	Light Pen Set. This active low signal is produced by the address decoder and used in the light pen logic (with the LPEN IN and LP CLR signals) to produce the LPEN STB signal.
LPEN STB	Light Pen Strobe. The light pen input (LPEN IN) generates the light pen strobe signal, which is sent to the Video Controller (VC). When the light pen is in use, this signal is used to latch the screen refresh address that the VC was accessing when the light pen was sensed. This tells the VC where the pen is located on the screen.
LPEN SW	Light Pen Switch. This signal from the light pen tells the CPU that the light pen is ON or OFF. When the pen is pressed against the CRT, the switch signal indicates the ON condition.
MEMR	Memory Read. This control signal from the processor or DMA Controller allows the CPU to read information from a memory location via a data bus. It is active low.
MEMW	Memory Write. This control signal from the processor or DMA Controller allows the CPU to write information from the data bus into a memory location. It is active low.
$\overline{\text{MOT A}}$, $\overline{\text{MOT B}}$	Drive Motor On. These active low signals are produced by the disk drive selection logic. They switch on the motor in the floppy disk drive unit that has been selected (SEL A or SEL B).
NMI	NonMaskable Interrupt. This active high signal causes the CPU to immediately stop its present operation and go to a routine specified for use when a problem occurs in the operation of the 8087 Numeric Processor (see NP INT below).
NP INT	Numeric Processor Interrupt. When the 8087 Numeric Processor has a problem in executing an instruction it has been given, it generates this signal and sends it to the NonMaskable Interrupt logic. This, in combination with other signals, tells the CPU that an error has occurred and vectors the processor to the appropriate error-handling routine. This is an active high signal.
NP INST	Numeric Processor Installed. Switch S1-1 (Desktop PC) or S2-1 (Portable PC) is the source of this signal. It tells the CPU and the NonMaskable Interrupt logic that the 8087 Numeric Processor is installed. When this switch is OFF, the system is configured to operate with the 8087 installed.
OSC	Oscillator. This is a high-speed clock signal that is provided to the expansion slots by the clock generator. Its frequency is the same as that of the clock generator crystal (14.318 MHz).
OUT0	Output 0. This output from the Programmable Interval Timer is a series of pulses that produces the highest-priority interrupt request (IRQ0) going to the interrupt controller. It causes the processor to execute a routine that updates the time of day clock.
OUT1	Output 1. When enabled by software, this output line from the Programmable Interval Timer causes a Direct Memory Access request (DRQ0). This request signals the DMA Controller that a device connected to one of the expansion slots needs a DMA transfer for memory refresh purposes.

OUT2	Output 2. The OUT2 signal from the Programmable Interval Timer is sent to the speaker driver circuitry. It provides the "beep" tone frequency for the speaker.
PCLK	Programmable Interval Timer Clock. This clock operates at one-half of the system clock frequency. It is sent to the Programmable Interval Timer (PIT) by the clock generator. It is divided further to provide the frequencies needed for the three OUT lines from the PIT.
PLL	Phase-Lock Loop signal. This is used to synchronize the hard disk drive. It receives a buffered INDEX signal from the disk drive every 16.67 ms.
PPI CS	Programmable Peripheral Interface Chip Select. This is an active low signal from the address decoder that selects the Programmable Peripheral Interface chip.
RAS0, RAS1	Row Address Select. These signals are used to access the rows of cells in the system memory. With the Column Address Select (CAS) signals, these allow the CPU or Video Controller to access any individual cell in the RAM. The CAS signals are produced in the memory row and column select logic, and go to the system memory.
RD DATA	Read Data. This is the line used to transfer data from the floppy disk to the Floppy Disk Controller. Data is separated from the clock pulses by the data separator Phase-Lock Loop and sent to the Floppy Disk Controller for transmission to the data bus.
RDY/WAIT	Ready/Wait. This signal is sent to the clock generator by the Bus Arbitrator. It controls the generation of the READY signal to the CPU. (This active high signal is similar to the DMA RDY signal.)
READY	Ready. This signal places the CPU in a waiting state when necessary to synchronize its operation with that of slower memory or peripheral devices. When this signal is high, the CPU is in a waiting state.
RES	System Reset. This active low signal is generated when the Reset switch is pressed. It causes the clock generator to send a RESET signal to the CPU.
RESET	Reset. This signal goes from the clock generator to the CPU. It causes the CPU to immediately stop what it is doing and return to the booting sequence. This active high signal is controlled by the reset switch.
S0, S1, S2	CPU Status Signals. In the maximum mode, the 8088 CPU uses these three signal lines to send coded information to the Bus Controller and Bus Arbitrator. As a result of these signals, the Bus Controller generates the control bus signals and sends the INTA signal to the Interrupt Controller in acknowledgement of an IRQ. These signals also cause the Bus Arbitrator to send the HLDA signal to the Direct Memory Access Controller.
SEL A, SEL B	Disk Drive Select. These active low signals are used to select floppy disk drive "A" or "B". They are used with the MOT A and MOT B signals. They come from the disk drive selection logic.
SER VID	Serial Video. Shift registers receive parallel character information from character ROMs. They convert it to serial video and send it to the video process logic. This signal is used to produce the video signals that drive the CRT.

$\overline{\text{SIDE 1}}$	Side 1. This active low signal from the Floppy Disk Controller to the disk drive tells the drive unit if the read or write operation is to be performed on side Ø or side 1 of the double-sided disk.
$\overline{\text{STEP}}$	Step. This active low signal consists of a series of pulses each of which causes the read/write head in the disk drive unit to step inward or outward by one track. The direction of travel is determined by the DIR signal.
TC	Terminal Count. The Direct Memory Access Controller (DMAC) sends this signal to a device that it has been servicing to indicate that the transfer is complete. The DMAC sends out an active low "End Of Process" signal (EOP). This is used by an inverter to generate the active high TC signal that goes to the Floppy Disk Controller and expansion slots.
$\overline{\text{TIC CS}}$	Time Interval Controller Chip Select. This signal is used to select the Programmable Interval Timer. It comes from the address decoder and it is active low.
$\overline{\text{TRKØ}}$	Track ØØ. This active low signal is generated by a sensor in the disk drive unit when the read/write head steps out to the outermost track (ØØ) on the disk. The Floppy Disk Controller uses it as a reference for calculating head position.
VSYNC	Vertical Synchronization. The VSYNC signal is produced by the Video Controller and sent through an inverter to the video connector.
WR CLK	Write Clock. This is a 1-MHz clock that is used for floppy disk read and write operations.
WR DATA	Write Data. The WR DATA line transfers serial data from the Floppy Disk Controller to the read/write head in the disk drive unit. Data to be written onto the disk is processed by the write precompensation logic before being sent to the disk drive.
$\overline{\text{WR GATE}}$	Write Gate. This signal determines which operation is to be performed: a read or a write. If this signal is high, read will occur. If it is low, write will occur.
$\overline{\text{WR NMI REG}}$	Write NonMaskable Interrupt Register. This active low signal that comes from the Address Decoder enables the NonMaskable Interrupt logic.
$\overline{\text{WR PROT}}$	Write-Protected. This is an active low signal produced by a sensor in the disk drive unit. If the disk in the drive is write-protected, this signal inhibits all write operations.
2M	2M Timing Signal. This timing signal is produced by a flip-flop in the video timing logic and processed by an inverter and gate to produce both positive and negative forms. It is used by the multiplexers in the video control logic to determine the times when the Video Controller or the CPU is allowed to access the system memory. Both cannot access memory at the same time.
32M	32M Timing Signal. This is a 34.37-MHz clock signal produced by a crystal oscillator and inverter circuit. It is used to produce the RAS and AMUX signals. It is also used by shift registers to convert parallel video information from the character generator ROMs into the SER VID signal.

Appendix D
BIOS ROM LISTING

```
;--------------------------------------------------------------------------
;EQUATES
;--------------------------------------------------------------------------
PORT_A          EQU     60H             ;8255 Port A address
PORT_B          EQU     61H             ;8255 Port B address
PORT_C          EQU     62H             ;8255 Port C address
CMD_PORT        EQU     63H             ;Command Port address
INTA00          EQU     20H             ;8259 Port
INTA01          EQU     21H             ;8259 Port
EOI             EQU     20H             ;End of Interrupt command
TIMER           EQU     40H             ;8253 Base address
TIMER0          EQU     40H             ;8253 Timer/Counter 0 Port address
TIM_CTL         EQU     43H             ;8253 Timer Control Port address
TMINT           EQU     1               ;Timer 0 Interrupt Received Mask
DMA08           EQU     8               ;DMA Status Register Port address
DMA             EQU     0               ;DMA Channel 0 Address Register Port address
MAX_PERIOD      EQU     540H            ;
MIN_PERIOD      EQU     410H            ;
KBD_IN          EQU     60H             ;Keyboard Data in Address Port
KBDINT          EQU     2               ;Keyboard Interrupt Mask
KB_DATA         EQU     60H             ;Keyboard Scan Code Port
KB_CTL          EQU     61H             ;Control Bits for Keyboard Sense Data
SCREENSEG       EQU     0B000H          ;Monochrome Screen Segment
COLORSEG        EQU     0B800H          ;Color Screen Segment
;--------------------------------------------------------------------------
;8088 INTERRUPT LOCATIONS
;--------------------------------------------------------------------------
ABSO            SEGMENT AT 0
STG_LOCO        LABEL   BYTE
                ORG     2*4
NMI_PTR         LABEL   WORD
                ORG     5*4
INT5_PTR        LABEL   WORD
                ORG     8*4
INT_ADDR        LABEL   WORD
INT_PTR         LABEL   DWORD
                ORG     10H*4
VIDEO_INT       LABEL   WORD
                ORG     1DH*4
PARM_PTR        LABEL   DWORD   ;Pointer to video parameters
                ORG     1EH*4
DISK_POINTER    LABEL   DWORD
                ORG     1FH*4
EXT_PTR         LABEL   DWORD   ;Pointer to extension
                ORG     7C00H
BOOT_LOCN       LABEL   FAR
ABSO            ENDS
```

```
;--------------------------------------------------------------------------
;STACK — USED DURING INIT. ONLY
;--------------------------------------------------------------------------
STACK           SEGMENT AT 30H
                DW      128 DUP (?)
TOS             LABEL   WORD
STACK           ENDS
;--------------------------------------------------------------------------
;ROM BIOS DATA AREAS
;--------------------------------------------------------------------------
DATA            SEGMENT AT 40H
RS232_BASE      DW      4 DUP (?)       ;Address of RS232 adapters
PRINTER_BASE    DW      4 DUP (?)       ;Address of printers
EQUIP_FLAG      DW      ?               ;Installed hardware
MFG_TST         DB      ?               ;Initialization flag
MEMORY_SIZE     DW      ?               ;Total memory size in K bytes
IO_RAM_SIZE     DW      ?               ;Memory in I/O Channel in K bytes
;--------------------------------------------------------------------------
;KEYBOARD DATA AREAS
;--------------------------------------------------------------------------
KB_FLAG         DB      ?
;--------SHIFT FLAG EQUATES WITHIN KB FLAG
INS_STATE       EQU     80H             ;Insert state is active
CAPS_STATE      EQU     40H             ;Caps Lock state has been toggled
NUM_STATE       EQU     20H             ;Num Lock state has been toggled
SCROLL_STATE    EQU     10H             ;Scroll Lock state has been toggled
ALT_SHIFT       EQU     08H             ;Alternate shift key depressed
CTL_SHIFT       EQU     04H             ;Control shift key depressed
LEFT_SHIFT      EQU     02H             ;Left shift key depressed
RIGHT_SHIFT     EQU     01H             ;Right shift key depressed
KB_FLAG 1       DB      ?               ;Second byte of keyboard status
INS_SHIFT       EQU     80H             ;Insert key depressed
CAPS_SHIFT      EQU     40H             ;Caps Lock key depressed
NUM_SHIFT       EQU     20H             ;Num Lock key depressed
SCROLL_SHIFT    EQU     10H             ;Scroll Lock key depressed
HOLD_STATE      EQU     08H             ;Suspend key has been toggled
ALT_INPUT       DB      ?               ;Storage for alternate keypad entry
BUFFER_HEAD     DW      ?               ;Pointer to head of keyboard buffer
BUFFER_TAIL     DW      ?               ;Pointer to tail of keyboard buffer
KB_BUFFER       DW      16 DUP (?)      ;Room for 15 entries
KB_BUFFER_END   LABEL   WORD
;--------HEAD = TAIL INDICATES BUFFER EMPTY CONDITION
NUM_KEY         EQU     69              ;Scan code for Num Lock key
SCROLL_KEY      EQU     70              ;Scroll Lock key
ALT_KEY         EQU     56              ;Alternate Shift Key
CTL_KEY         EQU     29              ;Control key
CAPS_KEY        EQU     58              ;Caps Lock key
LEFT_KEY        EQU     42              ;Left Shift key
RIGHT_KEY       EQU     54              ;Right Shift key
INS_KEY         EQU     82              ;Insert key
DEL_KEY         EQU     83              ;Delete key
```

```
;
;DISKETTE DATA AREAS
SEEK_STATUS     DB      ?               ;Drive recalibration status
                                        ;Bit 3-0 Drive 3-0 needs recall before
                                        ;next seek if bit = 0
INT_FLAG        EQU     080H            ;Interrupt occurrence flag
MOTOR_STATUS    DB      ?               ;Motor status
                                        ;Bit 3-0 Drive 3-0 is running
                                        ;Bit 7 operation is write, requires delay
MOTOR_COUNT     DB      ?               ;Time-out counter for drive turnoff
MOTOR_WAIT      EQU     37              ;Two seconds of count for motor off
DISKETTE_STATUS DB      ?               ;Single byte of return code information
TIME_OUT        EQU     80H             ;Attachment failed to respond
BAD_SEEK        EQU     40H             ;Seek operation failed
BAD_NEC         EQU     20H             ;NEC controller failed
BAD_CRC         EQU     10H             ;Bad CRC on diskette read
DMA_BOUNDARY    EQU     09H             ;Attempt to DMA across 64K boundary
BAD_DMA         EQU     08H             ;DMA overrun on operation
RECORD_NOT_FND  EQU     04H             ;Requested sector not found
WRITE_PROTECT   EQU     03H             ;Write attempt on protected disk
BAD_ADDR_MARK   EQU     02H             ;Address mark not found
BAD_CMD         EQU     01H             ;Bad command requested
NEC_STATUS      DB      7 DUP (?)       ;Status bytes from NEC
;
;VIDEO DISPLAY DATA AREA
CRT_MODE        DB      ?               ;Current CRT mode
CRT_COLS        DW      ?               ;Number of columns on screen
CRT_LEN         DW      ?               ;Length of Regen in bytes
CRT_STRT        DW      ?               ;Starting address in Regen buffer
CURSOR_POSN     DW      8 DUP (?)       ;Cursor for each of up to 8 pages
CURSOR_MODE     DW      ?               ;Current cursor mode setting
ACTIVE_PAGE     DB      ?               ;Current page being displayed
ADDR_6845       DW      ?               ;Base address for active display card
CRT_MODE_SET    DB      ?               ;Current setting of the 3 x 8 register
CRT_PALETTE     DB      ?               ;Current palette setting color card
;
;TIMER DATA AREAS
                ORG     06CH
TIMER_LOW       DW      ?               ;Low word of timer count
TIMER_HIGH      DW      ?               ;High word of timer count
TIMER_OFL       DB      ?               ;Timer rolled over since last read
; COUNTS_SEC    EQU     18
; COUNTS_MIN    EQU     1092
; COUNTS_HOUR   EQU     65543
; COUNTS_DAY    EQU     1573040 = 1800B0H
;
;SYSTEM DATA AREA
BIOS_BREAK      DB      ?               ;Bit 7 = 1 if Break key pressed
RESET_FLAG      DW      ?               ;Word = 1234H if keyboard reset under way
DATA            ENDS
```

```
;
;EXTRA DATA AREA
;
XXDATA          SEGMENT  AT 50H
STATUS_BYTE     DB       ?
XXDATA          ENDS
;
;VIDEO DISPLAY BUFFER
;
VIDEO_RAM       SEGMENT  AT 0B800H
REGEN           LABEL    BYTE
REGENW          LABEL    WORD
                DB       16384 DUP   (?)
VIDEO_RAM       ENDS
;
;ROM RESIDENT CODE
;
DMYCODE SEGMENT
CODE    EQU     0F000H                  ;Segment location
        ORG     0E000H

        DB      'Copyright 1983 Corona Data Systems'

;-------------------------------------------------------INTERRUPT 5H
;PRINT_SCREEN
;       This interrupt prints what is on the screen to a device. When this routine is invoked, the cursor
;       position is saved and then restored upon completion. The routine is intended to run with
;       interrupts enabled. If a subsequent print screen key is depressed during the time this routine is
;       printing, it will be ignored.
;   Address 50:0 contains the status of the print screen:
;
;   50:0    = 0     Either print screen has not been called, or upon return from a call this indicates a
;                   successful operation.
;
;   50:0    = 1     Print screen is in progress.
;
;   50:0    = 0FFH  Error encountered during printing.
;-----------------------------------------------------------------
PRINT_SCREEN    PROC    FAR
PRINT_SCREEN    ENDP

;-------------------------------------------------------INTERRUPT 9H
; This is the hardware keyboard interrupt routine.
;-----------------------------------------------------------------
KB_INT          PROC    FAR
KB_INT          ENDP
```

INTERRUPT 10H

```
;VIDEO IO
;       These routines provide,the CRT interface.
;       The following functions are provided:
;  AH = 0   Set mode AL contains mode value
;           AL = 0 40 x 25 BW (power on default)
;           AL = 1 40 x 25 COLOR
;           AL = 2 80 x 25 BW
;           AL = 3 80 x 25 COLOR
;           Graphic Modes
;           AL = 4 320 x 200 COLOR
;           AL = 5 320 x 200 BW
;           AL = 6 640 x 200 BW
;           CRT Mode
;           AL = 7 80 x 25 BW card (used internal to video only)
;           NOTE: BW modes operate same as color modes, but colorburst is not enabled.
;  AH = 1   Set cursor type
;           CH = Bits 0-4, start of line for cursor
;           NOTE: Hardware will always cause blink. Setting bit 5 or 6 will cause erratic blinking
;           or no cursor at all.
;           CL = Bits 0-4, end of line for cursor
;  AH = 2   Set cursor position
;           DH, DL = Row, column (0,0 is upper left)
;               BH = Page number (must be 0 for graphics mode)
;  AH = 3   Read cursor position
;           BH = Page number (must be 0 for graphics mode)
;           On exit DH, DL = Row, column of current cursor.
;                   CH, CL = Cursor mode currently set
;  AH = 4   Read light pen position
;           On exit AH = 0 Light pen switch no down/not triggered
;                   AH = 1 Valid light pen value in registers
;              DH, DL = Row, column of character LP position.
;                  CH = Raster line (0 - 199)
;                  BX = Pixel column (0 - 319, 639)
;  AH = 5   Select active display page (valid only for alpha modes)
;           AL = New page value (0 - 7 for modes 0, 1; 0 -3  for modes 2, 3)
;  AH = 6   Scroll active page up
;           AL      = Number of lines, input lines blanked at bottom of window
;           AL      = 0 means blank entire window
;           CH, CL  = Row, column of upper left corner of scroll
;           DH, DL  = Row, column of lower right corner of scroll
;           BH      = Attribute to be used on blank line
;  AH = 7   Scroll active page down
;           AL      = Number of lines, input lines blanked at top of window
;           AL      = 0 means blank entire window
;           CH, CL  = Row, column of upper left corner of scroll
;           DH, DL  = Row, column of lower right corner of scroll
;           BH      = Attribute to be used on blank line
```

```
;
;
;  Character Handling Routines
;  AH = 8  Read attribute/character at current cursor position
;          BH = Display page (valid for alpha modes only)
;          On exit AL = Character read
;                  AH = Attribute of character read (alpha modes only)
;  AH = 9  Write attribute/character at current cursor position
;          BH    = Display page (valid for alpha modes only)
;          CX    = Count of characters to write
;          BL    = Attribute of character (alpha mode) or
;                  color of character (graphic mode)
;          See note on write dot for 7 of BL = 1.
;  AH =10  Write character only at current cursor position
;          BH    = Display page (valid for alpha modes only)
;          CX    = Count of characters to write
;          AL    = Character to write
;
;

;  For read/write character interface while in graphics mode, the characters are formed from a
;  character generator image maintained in the system ROM. Only the first 128 characters are
;  contained there. To read/write the second 128 characters you must initialize the pointer to the 1K
;  byte table that contains the code points for the second 128 characters (128-255).
;
;  For write character interface in graphics mode, the replication factor contained in CX on entry will
;  produce valid results only for characters contained in the same row. Continuation to succeeding
;  lines will not produce correctly.
;
;
;  Graphics Interface
;  AH = 11 Set color palette
;          BH    = Palette color ID being sent (0- 127)
;          BL    = Color value to be used with that color ID
;          NOTE: For the current color card, this entry point has meaning only for 320x 200 graphics.
;          COLOR ID  = 0 selects the background color (0- 15)
;          COLOR ID  = 1 selects the palette to be used:
;                      0 = Green, red, yellow for colors 1, 2, 3
;                      1 = Cyan, magenta, white for colors 1, 2, 3
;          In 40x 25 or 80x 25 alpha modes, the value set for palette color 0 indicates the border color
;          to be used (values 0- 31, where 16-31 select the high intensity background set.
;  AH = 12 Write dot
;          DX = Row number
;          CX = Column number
;          AL = Color value
;               If bit 7 of AL = 1, then the color value is exclusive OR'd with the current contents of
;               the dot.
;  AH = 13 Read dot
;          DX = Row number
;          AL = Returns the dot read
;
```

```
;
;   ASCII Teletype Routine for Output
;   AH = 14   Write teletype
;             AL = Character to write
;             BL = Foreground color in graphics mode
;             BH = Display page in alpha mode
;           NOTE: Screen width is controlled by previous mode set.
;
;   AH = 15 Current video state
;             AL = Mode currently set (see AH = 0 for explanation)
;             AH = Number of character columns on screen
;             BH = Current active display page
;
;   CS, SS, DS, ES, BX, CX, DX are preserved during call.
;   All others are destroyed.
; ------------------------------------------------------------------------
VIDEO_IO    PROC    NEAR
VIDEO_IO    ENDP
;--------Tables for use in setting of mode
VIDEO_PARMS
            LABEL   BYTE
;--------INIT_TABLE
            DB      38H,28H,2DH,0AH,1FH,6,19H       ;Set up for 40 x 25
            DB      1CH,2,7,6,7
            DB      0, 0, 0, 0

            DB      71H,50H,5AH,0AH,1FH,6,19H       ;Set up for 80 x 25
            DB      1CH,2,7,6,7
            DB      0, 0, 0, 0

            DB      38H,28H,2DH,0AH,7FH,6,64H       ;Set up for graphics
            DB      70H,2,1,6,7
            DB      0, 0, 0, 0

VTABLE      DB      65H,50H,51H,0AH,1AH,0,19H       ;Set up for 80 x 25 BW card

            DB      19H,2,0CH,0AH,0BH
            DB      0, 0, 0, 0

M5          LABEL   WORD                            ;Table of lengths
            DW       2048                           ;40 x 25
            DW       4096                           ;80 x 25
            DW      16384                           ;Graphics
            DW      16384
;--------COLUMNS
M6          LABEL   BYTE
            DB      40,40,80,80,40,40,80,80
;--------C REG TAB
M7          LABEL   BYTE                            ;Table of mode sets
            DB      2CH,28H,2DH,29H,2AH,2EH,1EH,28H

; ------------------------------------------------------------------------
```

```
; ---------------------------------------INTERRUPT 11H---------------------------------------
; EQUIPMENT
;       This routine attempts to determine what optional devices are attached to the system.
;    Input
;         No registers
;         The EQUIP_FLAG variable is set during the power-on diagnostics
;         using the following hardware assumptions:
;         PORT 60   = Low-order byte of equipment
;         PORT 3FA = Interrupt ID register of 8250
;                    Bits 7-3 are always 0
;         PORT 378 = Output port of printer
;                    (8255 port that can be read as well as written)
;    Output
;       AX is set, bit significant, to indicate attached I/O
;            Bits 15,14 = Number of printers attached
;                Bit 13 = Not used
;                Bit 12 = Game I/O attached
;           Bits 11,10,9 = Number of RS232 cards attached
;                  Bit 8 = Not used
;              Bits 7,6 = Number of diskette drives
;                         00=1, 01=2, 10=3, 11=4, only if bit 0=1
;              Bits 5,4 = Initial video mode
;                         00 = Not used
;                         01 = 40x25 BW using color card
;                         10 = 80x25 BW using color card
;                         11 = 80x25 BW
;              Bits 3,2 = Planar RAM size
;                         00=16K, 01=32K, 10=48K, 11=64K
;                  Bit 1 = Not used
;                  Bit 0 = IPL from diskette -- indicates there are diskette
;                         drives on the system
;       No other registers affected
; -------------------------------------------------------------------------------------------

EQUIPMENT       PROC    FAR
EQUIPMENT       ENDP

CASSETTE_IO     PROC    FAR
                STC
                MOV     AH,80H          ;Any call to CASSETTE_IO returns
                IRET                    ;an error condition.
CASSETTE_IO     ENDP
```

```
;--------------------------------------------INTERRUPT 12H--------------------------------------------
; MEMORY_SIZE_DETERMINE
;       This routine determines the amount of memory in the system as represented by the switches on
;       the planar. It will not necessarily recognize memory that is not contiguous.
;    Input
;       No register
;       The MEMORY_SIZE variable is set during power-on diagnostics according to the following
;       hardware assumptions:
;       PORT 60, bits 3,2 = Amount of RAM
;                                   00 =  16K  RAM
;                                   01 =  32K  RAM
;                                   10 =  48K  RAM
;                                   11 =  64K  RAM
;       PORT 62, bits 3-0, indicates amount of I/O RAM in 32K increments
;                         e.g., 0000 =  No  RAM  in  I/O channel
;                               0010 =  64K  RAM  in  I/O channel, etc.
;    Output
;       AX = Number of contiguous 1K blocks of memory
;------------------------------------------------------------------------------------------------------
MEMORY_SIZE_DETERMINE   PROC    FAR
MEMORY_SIZE_DETERMINE   ENDP
;--------------------------------------------INTERRUPT 13H--------------------------------------------
; DISKETTE_IO
;       This interface provides access to the 5 1/4" diskette drives.
;    Input
;       AH = 0  Reset diskette system. Hard reset to NEC, prepare command, recall read on all drives
;       AH = 1  Read the status of the system into AL.
;               Diskette status from last opened drive is used
;       Registers for read/write/verify/format
;                     DL = Drive number (0-3 allowed, value checked)
;                     DH = Head number (0-1 allowed, value not checked)
;                     CH = Track number (0-39 allowed, value not checked)
;                     CL = Sector number (1-8 allowed, value not checked)
;                     AL = Number of sectors (max = 8, value not checked)
;                  ES:BX = Address of buffer (not required for verify)
;       AH = 2 Read the desired sectors into memory
;       AH = 3 Write the desired sectors into memory
;       AH = 4 Verify the desired sectors
;       AH = 5 Format the desired track
;               For the format operation, the buffer pointer (ES, BX) must point
;               to the collection of desired address fields for the track. Each
;               field is composed of 4 bytes (c,h,r,n), where:
;               c = track number, h = head number, r = sector number,
;               n = number of bytes per sector (00=128, 01=256, 02=512, etc.).
;               This information is used to find the requested sector during
;               read/write access.
;    DATA VARIABLE -- DISK POINTER
;       Double word pointer to the current set of disk parameters
;    Output
;       AH = Status of operation
;            Status bits are defined in the equates for DISKETTE STATUS
;            variable in the data segment of this module
;       CY = 0  Successful operation (AH = 0 on return)
;       CY = 1  Failed operation (AH has error reason)
```

```
;       For read/write/verify
;            DS,BX,DX,CH,CL preserved
;       AL = Number of sectors actually read
;            NOTE: AL may not be correct if time-out error occurs.
;       NOTE: If an error is reported by the diskette code, the appropriate action is to reset the diskette,
;       then retry the operation. On read access, no motor start delay is taken, so that three retries are
;       required on reads to ensure that the problem is not due to motor start-up.
;--------------------------------------------------------------------------------
DISKETTE_IO     PROC    FAR
DISKETTE_IO     ENDP

;--------------------------------------------------------------------------------
; DISK_BASE
;       This is the set of parameters required for diskette operation. They are pointed at by the data
;       variable DISK_POINTER. To modify the parameters, build another parameter block, and point
;       at it.
;--------------------------------------------------------------------------------
DISK_BASE       LABEL   BYTE
    DB          11001111B       ;SRT=C, HD UNLOAD=0F (first specified byte)
    DB          2               ;HD LOAD +1, mode = DMA (second specified byte)
    DB          MOTOR_WAIT      ;Wait after operation until motor off
    DB          2               ;512 bytes/sector
    DB          8               ;EOT (last sector on track)
    DB          2AH             ;Gap length
    DB          0FFH            ;DTL
    DB          50H             ;Gap length for format
    DB          0F6H            ;Fill byte for format
    DB          25              ;Head settle time (milliseconds)
    DB          4               ;Motor start time (1/8 seconds)

;--------------------------------------------INTERRUPT 14H--------------------------------------------
; RS232_IO
;       This routine provides byte stream I/O to the communications port according to the parameters:
;       AH = 0 Initialize the communications port
;            AL has parameters for initialization
;          7       6       5       4       3       2       1       0
;        ---Baud Rate---         --Parity--      Stop Bit  --Word Length--
;          000 - 110               X0 - None       0 - 1       10 - 7 Bits
;          001 - 150               01 - Odd        1 - 2       11 - 8 Bits
;          010 - 300               11 - Even
;          011 - 600
;          100 - 1200
;          101 - 2400
;          110 - 4800
;          111 - 9600
;          On return, conditions set as in call to comm status (AH=3).
```

```
;       AH = 1  Send the character in AL over the COMMO line.
;               AL register is preserved.
;               On exit, bit 7 of AH is set if the routine was unable to transmit the byte of data
;               over the line. The remainder of AH is set as in a status request, reflecting the
;               current status of the line.
;       AH = 2  Receive a character in AL from the COMMO  line before returning to caller.
;               On exit, AH has the current line status, as set by the status routine, except that
;               the only bits left on are the error bits (7,4,3,2,1). In this case, the time-out bit
;               indicates Data Set Ready was not received. Thus, AH is nonzero only when an
;               error occurred.
;       AH = 3  Return the communications port status in AX
;               AH contains the control line status
;               Bit 7 = Time out
;               Bit 6 = Transmitter shift register empty
;               Bit 5 = Transmitter holding register empty
;               Bit 4 = Break detected
;               Bit 3 = Framing error
;               Bit 2 = Parity error
;               Bit 1 = Overrun error
;               Bit Ø = Data Ready
;        AL contains the modem status
;               Bit 7 = Received line signal detect
;               Bit 6 = Ring indicator present
;               Bit 5 = Data set ready
;               Bit 4 = Clear to send
;               Bit 3 = Delta receive line signal detect
;               Bit 2 = Trailing edge ring detector
;               Bit 1 = Delta data set ready
;               Bit Ø = Delta clear to send
;       DX = Parameter indicating which RS232 card (Ø, 1 allowed).
;       Data Area RS232_BASE contains the base address of the 8250 on the card.
;       Location 400H contains up to four RS232 addresses possible.
;     Output
;       AX modified according to parameters of call
;       All others unchanged
;--------------------------------------------------------------------------------
A1              LABEL   WORD    ;Table of initial values
                DW      1047    ;110 Baud
                DW      768     ;150
                DW      384     ;300
                DW      192     ;600
                DW      96      ;1200
                DW      48      ;2400
                DW      24      ;4800
                DW      12      ;9600

;--------------------------------------------------------------------------------
RS232_IO        PROC    FAR
RS232_IO        ENDP
```

```
;--------------------------------------------INTERRUPT 16H--------------------------------------------
; Keyboard I/O
;       These routines provide keyboard support.
;    Input
;       AH = Ø  Read the next ASCII character struck from the keyboard.
;               Return the result in AL, scan code in AH.
;       AH = 1  Set the Z flag to indicate if an ASCII character is available to read.
;               ZF = 1  No code is available
;               ZF = Ø  Code is available
;               If ZF = Ø, the next character in the buffer to be read is in AX, and the entry remains in
;               the buffer.
;       AH = 2  Return the current shift status in the AL register.
;               The bit settings for this code are indicated in the equates for the KB_FLAG.
;    Output
;       As noted above, only AX and FLAGS are changed.
;       All registers are retained.
;-----------------------------------------------------------------------------------------------------
KEYBOARD_IO     PROC    FAR
KEYBOARD_IO     ENDP
;--------------------------------------------INTERRUPT 17H--------------------------------------------
; PRINTER I/O
;       This routine provides communication with the printer.
;       AH = Ø Print the character in AL.
;               On return, AH = 1 if the character could not be printed (time out).
;       Other bits set as on normal status call.
;       AH = 1 Initialize the printer port.
;               Returns with AH set with printer status.
;       AH = 2 Read the printer status into AH.
;                       Ø = Time out
;                     1-2 = Not used
;                       3 = I/O error
;                       4 = Selected
;                       5 = Out of paper
;                       6 = Acknowledge
;                       7 = Busy
;       DX = Printer to be used (Ø,1,2) corresponding to actual values in PRINTER_BASE area
;       Data area PRINTER_BASE contains the base address of the printer card(s) available (located at
;       beginning of data segment, 408H absolute, 3 words).
;    Registers
;       AH is modified
;       All others unchanged
;-----------------------------------------------------------------------------------------------------
PRINTER_IO      PROC    FAR
PRINTER_IO      ENDP

;--------------------------------------------INTERRUPT 19H--------------------------------------------
; BOOTSTRAP_LOADER
;       Track Ø, sector 1 is read into the boot location (segment Ø, offset 7CØØ), and control is
;       transferred there.
;-----------------------------------------------------------------------------------------------------
```

```
;--------------------------------------INTERRUPT 1AH--------------------------------------
; TIME_OF_DAY
;    This routine allows the clock to be set/read.
;    Input
;       AH = Ø Read the current clock setting
;              Returns CX = High portion of count
;                      DX = Low portion of count
;                      AL = Ø if timer has not passed 24 hours since last read
;                        <>Ø if on another day
;       AH = 1 Set the current clock
;              CX = High portion of count
;              DX = Low portion of count
;       NOTE: Counts occur at the rate of 1193180/65536 counts/sec
;              (or about 18.2 per second -- see equates below)
;-----------------------------------------------------------------------------------------
TIME_OF_DAY     PROC    FAR
TIME_OF_DAY     ENDP

;-----------------------------------------------------------------------------------------
; TIMER_INT
;       This routine handles the timer interrupt from channel Ø of the 8253 timer. Input frequency is
;       1.19318 MHz, and the divisor is 65536, resulting in approximately 18.2 interrupts every second.
;
;       The interrupt handler maintains a count of interrupts since power-on time, which may be used to
;       establish time of day. The interrupt handler also decrements the motor control count of the
;       diskette, and when it expires, will turn off the diskette motor, and reset the motor running flags.
;
;       The interrupt handler will also invoke a user routine through interrupt 1CH at every time tick. You
;       must code a routine and place the correct address in the vector table.
;-----------------------------------------------------------------------------------------
TIMER_INT       PROC    FAR
TIMER_INT       ENDP

;-----------------------------------------------------------------------------------------
; VECTOR_TABLE
;       These are the vectors that are moved into the 8086 interrupt area during power-on.

VECTOR_TABLE    LABEL WORD                      ;Vector table for move to interrupts
                DW    OFFSET TIMER_INT          ;Interrupt 8
                DW    CODE

                DW    OFFSET KB_INT             ;Interrupt 9
                DW    CODE

                DD    Ø                         ;Interrupt A
                DD    Ø                         ;Interrupt B
                DD    Ø                         ;Interrupt C
                DD    Ø                         ;Interrupt D
                DW    OFFSET DISK_INT           ;Interrupt E
                DW    CODE

                DD    Ø                         ;Interrupt F

                DW    OFFSET VIDEO_IO           ;Interrupt 10H
                DW    CODE
```

```
                DW      OFFSET EQUIPMENT                ;Interrupt 11H
                DW      CODE

                DW      OFFSET MEMORY_SIZE_DETERMINE;Interrupt 12H
                DW      CODE

                DW      OFFSET DISKETTE_IO              ;Interrupt 13H
                DW      CODE

                DW      OFFSET RS232_IO                 ;Interrupt 14H
                DW      CODE

                DW      OFFSET CASSETTE_IO              ;Interrupt 15H (unused)
                DW      CODE

                DW      OFFSET KEYBOARD_IO              ;Interrupt 16H
                DW      CODE

                DW      OFFSET PRINTER_IO               ;Interrupt 17H
                DW      CODE

                DW      OFFSET DUMMY_RETURN             ;Interrupt 18H (unused)
                DW      CODE

                DW      OFFSET BOOT_STRAP               ;Interrupt 19H
                DW      CODE

                DW      OFFSET TIME_OF_DAY              ;Interrupt 1AH, time of day
                DW      CODE

                DW      OFFSET DUMMY_RETURN             ;Interrupt 1BH, keyboard
                                                        ;break address
                DW      CODE

                DW      OFFSET DUMMY_RETURN             ;Interrupt 1CH, timer break address
                DW      CODE

                DW      OFFSET VIDEO_PARMS              ;Interrupt 1DH, video parms
                DW      CODE

                DW      OFFSET DISK_BASE                ;Interrupt 1EH, disk parms
                DW      CODE

                DD      0                               ;Interrupt 1FH,
                                                        ;pointer to video extended character set
;--------------------------------------------------------------------------------
PRINT_SCREEN    PROC    FAR
PRINT_SCREEN    ENDP

DMYCODE         ENDS
                END
```

Appendix E
KEYBOARD CODES, CHARACTERS, AND FUNCTIONS

VALUE		CHARACTERS AND SYMBOLS		ASCII CONTROL CODE
HEX	DEC	SYMBOL	KEYSTROKES	SYMBOL
00	0	BLANK (NULL)	CTRL 2	NUL
01	1	☺	CTRL A	SOH
02	2	☻	CTRL B	STX
03	3	♥	CTRL C	ETX
04	4	♦	CTRL D	EOT
05	5	♣	CTRL E	ENQ
06	6	♠	CTRL F	ACK
07	7	•	CTRL G	BEL
08	8	◘	CTRL H, BACKSPACE, SHIFT BACKSPACE	BS
09	9	○	CTRL I	HT
0A	10	◙	CTRL J, CTRL ↵	LF
0B	11	♂	CTRL K	VT
0C	12	♀	CTRL L	FF
0D	13	♪	CTRL M ↵, SHIFT ↵	CR
0E	14	♫	CTRL N	SØ
0F	15	☼	CTRL O	S1
10	16	►	CTRL P	DLE
11	17	◄	CTRL Q	DC1
12	18	↕	CTRL R	DC2
13	19	‼	CTRL S	DC3
14	20	¶	CTRL T	DC4
15	21	§	CTRL U	NAK
16	22	▬	CTRL V	SYN
17	23	↨	CTRL W	ETB

VALUE		CHARACTERS AND SYMBOLS		ASCII CONTROL CODE
HEX	DEC	SYMBOL	KEYSTROKES	SYMBOL
18	24	↑	CTRL X	CAN
19	25	↓	CTRL Y	EM
1A	26	→	CTRL Z	SUB
1B	27	←	CTRL [, ESC, SHIFT ESC, CTRL ESC	ESC
1C	28	∟	CTRL \	FS
1D	29	↔	CTRL]	GS
1E	30	▲	CTRL 6	RS
1F	31	▼	CTRL–	US
20	32	BLANK (SPACE)	SPACEBAR, SHIFT SPACE CTRL SPACE, ALT SPACE	SPA
21	33	!	!	
22	34	"	"	
23	35	#	#	
24	36	$	$	
25	37	%	%	
26	38	&	&	
27	39	'	'	
28	40	(	(	
29	41	)	)	
2A	42	*	*	
2B	43	+	+	
2C	44	,	,	
2D	45	—	—	
2E	46	-	-	

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
2F	47	/	/
30	48	0	0
31	49	1	1
32	50	2	2
33	51	3	3
34	52	4	4
35	53	5	5
36	54	6	6
37	55	7	7
38	56	8	8
39	57	9	9
3A	58	:	:
3B	59	;	;
3C	60	<	<
3D	61	=	=
3E	62	>	>
3F	63	?	?
40	64	@	@
41	65	A	A
42	66	B	B
43	67	C	C
44	68	D	D
45	69	E	E
46	70	F	F
47	71	G	G
48	72	H	H
49	73	I	I
4A	74	J	J
4B	75	K	K

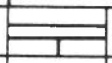
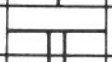
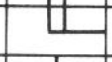
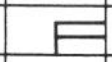
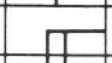
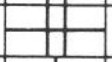
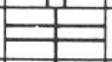
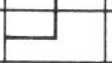
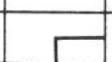
VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
4C	76	L	L
4D	77	M	M
4E	78	N	N
4F	79	O	O
50	80	P	P
51	81	Q	Q
52	82	R	R
53	83	S	S
54	84	T	T
55	85	U	U
56	86	V	V
57	87	W	W
58	88	X	X
59	89	Y	Y
5A	90	Z	Z
5B	91	[	[
5C	92	\	\
5D	93	]	]
5E	94	^	^
5F	95	_	_
60	96	`	`
61	97	a	a
62	98	b	b
63	99	c	c
64	100	d	d
65	101	e	e
66	102	f	f
67	103	g	g

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
68	104	h	h
69	105	i	i
6A	106	j	j
6B	107	k	k
6C	108	l	l
6D	109	m	m
6E	110	n	n
6F	111	o	o
70	112	p	p
71	113	q	q
72	114	r	r
73	115	s	s
74	116	t	t
75	117	u	u
76	118	v	v
77	119	w	w
78	120	x	x
79	121	y	y
7A	122	z	z
7B	123	{	{
7C	124	|	|
7D	125	}	}
7E	126	~	~
7F	127	△	CTRL ←
• • • 80 HEX - FF HEX ARE FLASHING			
80	128	Ç	ALT 128
81	129	ü	ALT 129
82	130	é	ALT 130
83	131	â	ALT 131

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
84	132	ä	ALT 132
85	133	à	ALT 133
86	134	å	ALT 134
87	135	ç	ALT 135
88	136	ê	ALT 136
89	137	ë	ALT 137
8A	138	è	ALT 138
8B	139	ï	ALT 139
8C	140	î	ALT 140
8D	141	ì	ALT 141
8E	142	Ä	ALT 142
8F	143	Å	ALT 143
90	144	É	ALT 144
91	145	æ	ALT 145
92	146	Æ	ALT 146
93	147	ô	ALT 147
94	148	ö	ALT 148
95	149	ò	ALT 149
96	150	û	ALT 150
97	151	ù	ALT 151
98	152	ÿ	ALT 152
99	153	Ö	ALT 153
9A	154	Ü	ALT 154
9B	155	Ç	ALT 155
9C	156	£	ALT 156
9D	157	¥	ALT 157
9E	158	Pts	ALT 158

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
9F	159	ƒ	ALT 159
A0	160	á	ALT 160
A1	161	í	ALT 161
A2	162	ó	ALT 162
A3	163	ú	ALT 163
A4	164	ñ	ALT 164
A5	165	Ñ	ALT 165
A6	166	ª	ALT 166
A7	167	º	ALT 167
A8	168	¿	ALT 168
A9	169	⌐	ALT 169
AA	170	¬	ALT 170
AB	171	½	ALT 171
AC	172	¼	ALT 172
AD	173	¡	ALT 173
AE	174	«	ALT 174
AF	175	»	ALT 175
B0	176	▒	ALT 176
B1	177	▒	ALT 177
B2	178	▓	ALT 178
B3	179	│	ALT 179
B4	180	┤	ALT 180
B5	181	╡	ALT 181
B6	182	╢	ALT 182
B7	183	╖	ALT 183
B8	184	╕	ALT 184

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
B9	185	╣	ALT 185
BA	186	║	ALT 186
BB	187	╗	ALT 187
BC	188	╝	ALT 188
BD	189	╜	ALT 189
BE	190	╛	ALT 190
BF	191	┐	ALT 191
C0	192	└	ALT 192
C1	193	┴	ALT 193
C2	194	┬	ALT 194
C3	195	├	ALT 195
C4	196	─	ALT 196
C5	197	┼	ALT 197
C6	198	╞	ALT 198
C7	199	╟	ALT 199
C8	200	╚	ALT 200
C9	201	╔	ALT 201
CA	202	╩	ALT 202
CB	203	╦	ALT 203
CC	204	╠	ALT 204
CD	205	═	ALT 205
CE	206	╬	ALT 206
CF	207	╧	ALT 207
D0	208	╨	ALT 208

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
D1	209		ALT 209
D2	210		ALT 210
D3	211		ALT 211
D4	212		ALT 212
D5	213		ALT 213
D6	214		ALT 214
D7	215		ALT 215
D8	216		ALT 216
D9	217		ALT 217
DA	218		ALT 218
DB	219		ALT 219
DC	220		ALT 220
DD	221		ALT 221
DE	222		ALT 222
DF	223		ALT 223
E0	224	α	ALT 224
E1	225	β	ALT 225
E2	226	γ	ALT 226
E3	227	π	ALT 227
E4	228	Σ	ALT 228
E5	229	σ	ALT 229
E6	230	μ	ALT 230
E7	231	τ	ALT 231
E8	232	Φ	ALT 232
E9	233	Θ	ALT 233
EA	234	Ω	ALT 234
EB	235	δ	ALT 235

VALUE		CHARACTERS AND SYMBOLS	
HEX	DEC	SYMBOL	KEYSTROKES
EC	236	∞	ALT 236
ED	237	ϕ	ALT 237
EE	238	ϵ	ALT 238
EF	239	$\cap$	ALT 239
F0	240	$\equiv$	ALT 240
F1	241	$\pm$	ALT 241
F2	242	$\geq$	ALT 242
F3	243	$\leq$	ALT 243
F4	244	$\int$	ALT 244
F5	245		ALT 245
F6	246	$\div$	ALT 246
F7	247	$\approx$	ALT 247
F8	248	$\circ$	ALT 248
F9	249	$\bullet$	ALT 249
FA	250	$\cdot$	ALT 250
FB	251	$\surd$	ALT 251
FC	252	η	ALT 252
FD	253	^{2}	ALT 253
FE	254	■	ALT 254
FF	255	BLANK	ALT 255

NOTE 1 The 3 digits after the ALT key must be typed from the numeric key pad. Character codes 128 through 255 can be entered in this fashion.

NOTE 2 For enhancements such as high intensity, reverse video, blinking, and underline, see Fig. 3-3.

KEYBOARD SCAN CODES

Key Designation	Scan Code in Hex	Key Designation*	Scan Code in Hex
Esc	01	\	2B
1	02	Z	2C
2	03	X	2D
3	04	C	2E
4	05	V	2F
5	06	B	30
6	07	N	31
7	08	M	32
8	09	,	33
9	0A	.	34
0	0B	/	35
-	0C	Shift (R)	36
=	0D	*(PrtSc)	37
Backspace	0E	Alt	38
Tab	0F	Spacebar	39
Q	10	Caps Lock	3A
W	11	F1	3B
E	12	F2	3C
R	13	F3	3D
T	14	F4	3E
Y	15	F5	3F
U	16	F6	40
I	17	F7	41
O	18	F8	42
P	19	F9	43
[	1A	F10	44
]	1B	Num Lock	45
Return	1C	Scroll Lock	46
Ctrl	1D	[7]	47
A	1E	[8]	48
S	1F	[9]	49
D	20	-	4A
F	21	[4]	4B
G	22	[5]	4C
H	23	[6]	4D
J	24	+	4E
K	25	[1]	4F
L	26	[2]	50
;	27	[3]	51
'	28	Ins	52
`	29	Del	53
Shift (L)	2A		

*Numbers enclosed in square brackets must be entered from the numeric keypad in Num Lock mode.

Appendix F
DESKTOP PC AND PORTABLE PC SYSTEM MEMORY MAP

START ADDRESS DECIMAL	START ADDRESS HEX	FUNCTION
0	00000	**System Memory on PCB**
64K	10000	128K Dynamic Memory
128K	20000	
192K	30000	128K Memory (optional)
256K	40000	
320K	50000	128K Memory (optional)
384K	60000	
448K	70000	128K Memory (optional)
512K	80000	
576K	90000	128K I/O Channel RAM Space
640K	A0000	
704K	B0000	**128K Reserved** Alphanumeric Screen 4K at B0000 Color/Graphics 16K at B8000
768K	C0000	
832K	D0000	Hard Disk Control at C8000
896K	E0000	**Reserved for 192K ROM**
960K	F0000	ROM BIOS 8K at FE000
1024K	FFFFF	

Note: PC monochrome graphics require 32K per graphic page, and pages 0 through 7 start at 00000H in the default mode. Starting address can be moved to 40000H using an internal jumper on the main PC board.

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34.37 MHz, see Oscillator
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8048, see Keyboard Microprocessor
8087, see Co-processor
8088, see Central Processing Unit
8237A, see DMA Controller
8250, see Universal Asynchronous Receiver-Transmitter
8253-5, see Programmable Interval Timer
8255-5, see Programmable Peripheral Interface
8259A, see Programmable Interrupt Controller
8284A, see Clock Generator
8288, see Bus Controller

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```
P P P   C C C          P P P   3 3 3   1   0 0 0   0 0 0
P   P   C              P   P       3   1   0   0   0   0
P P P   C       -----  P P P   3 3 3   1   0   0   0   0
P       C              P       3   1   0   0   0   0
P       C C C          P       3 3 3   1   0 0 0   0 0 0
```

Service bulletin

Nummer: Datum:

Onderwerp: Tips voor gebruik van uitbreidingskaarten in PC's.

Dit bulletin geldt voor P3101, P3102 en P3200.

Dit bulletin bevat:
1. Algemene inleiding.
2. I/O adressen, Interrupt- en DMA-kanalen.
3. Overzicht P3101 en P3102.
4. Overzicht P3200.

1. Algemene inleiding.

Uitbreidingskaarten voor PC's kunnen op vele plaatsen gekocht worden. Veelal heeft een gebruiker op de vrije markt een grote keuze van uitbreidingskaarten. Een aantal van deze kaarten kunnen nooit samen in een PC gebruikt worden omdat ze gebruik maken van de zelfde I/O-poorten, interrupt-lijnen of DMA-kanalen. Dit bulletin geeft een overzicht van de door PTIS geleverde uitbreidingskaarten en welke I/O-poorten, interrupt lijnen en DMA-kanalen gebruikt worden.

2. I/O adressen, Interrupt-lijnen en DMA-kanalen.

* I/O-poorten.

Zowel de P3101, P3102 als de P3200 beschikken in principe over 1024 I/O-poorten. De eerste 256 zijn gereserveerd voor de functies die zich op het moederbord bevinden. Van de overgebleven I/O-poorten zijn er een aantal gereserveerd voor standaard interfaces, zoals harddisk, foppy-disk, serie- en parallelle interfaces. De overige I/O-poorten kunnen door uitbreidingskaarten benut worden. Welke I/O-poorten er gebruikt worden bij vreemde uitbreidingskaarten is haast altijd in de bijgeleverde documentatie terug te vinden.

* Interrupt lijnen P3101 en P3102.

De P3101 en P3102 beschikken over een 8-tal interrupt lijnen. Deze lijnen zijn IRQ0 t/m IRQ7 genoemd.

IRQ0 Timer interrupt voor systeemtijd.
IRQ1 Keyboard interrupt.
IRQ2 Geen standaard funktie.
IRQ3 Gereserveerd voor COM2.
IRQ4 Interne serie interface COM1.
IRQ5 Harddisk controller.
(Indien geen harrdisk aanwezig, IRQ5 vrij beschikbaar.)
IRQ6 Floppy-disk controller.
IRQ7 Gereserveerd voor parallel interfaces (LPT1, en LPT2).
(De parallel interfaces gebruiken echter nooit de interrupt funkties. Hierdoor is IRQ7 ook vrij beschikbaar.)

De interrupt lijnen IRQ2 t/m IRQ7 worden naar de slots uitgevoerd.

* Interrupt lijnen P3200.

De P3200 beschikt over een 16-tal interrupt lijnen. Deze lijnen zijn IRQ0 t/m IRQ15 genoemd.

De interrupt lijnen worden alsvolgt gebruikt.

IRQ0 Timer interrupt voor systeemtijd.
IRQ1 Keyboard interrupt.
IRQ2 Cascade voor tweede interrupt controller.
IRQ3 Gereserveerd voor COM2.
IRQ4 Gereserveerd voor COM1.
IRQ5 Gereserveerd voor parallel interface LPT2.
IRQ6 Floppy-disk controller.
IRQ7 Gereserveerd voor parallel interface LPT1.

(De parallel interfaces gebruiken echter nooit de interrupt funkties. Hierdoor zijn IRQ5 en IRQ7 vrij beschikbaar.)

IRQ8 Interrupt van interne klok-kalender.
IRQ9 Geen standaard funktie.
IRQ10 Geen standaard funktie.
IRQ11 Geen standaard funktie.
IRQ12 Geen standaard funktie.
IRQ13 Co-processor 80287.
IRQ14 Harddisk controller.
IRQ15 Geen standaard funktie.

Naar een 8 bits slot worden de interrupt lijnen IRQ3 t/m IRQ7 en IRQ9 doorverbonden. Naar een 16 bits slot gaan de interrupt lijnen IRQ3 t/m IRQ7, IRQ9 t/m IRQ12, IRQ14 en IRQ15.

Het 8 bits slot is compatibel met het slot in de P3101 en P3102. Fysiek zit IRQ9 op de plaats waar bij een P3101 of P3102 IRQ2 geplaatst is. De BIOS-ROM beschouwt hier een interrupt van IRQ9 als een interrupt van IRQ2.

* DMA-kanalen P3101 en P3102.

De P3101 en P3102 beschikken over een 4-tal DMA-kanalen. Deze DMA-kanalen zijn DRQ0 t/m DRQ3 genoemd.

De DMA-kanalen worden alsvolgt gebruikt.

DRQ0 DMA-refresh.
DRQ1 Geen standaard funktie.
DRQ2 Floppy-disk controller.
DRQ3 Harddisk controller. (Alleen Western Digital controller)
(Indien niet aanwezig, dan is DRQ3 vrij te gebruiken.)

De DMA-kanalen DRQ1 t/m DRQ3 worden naar de slots geleid.

* DMA-kanalen P3200.

De P3200 beschikt over een 8-tal DMA-kanalen. Deze DMA-kanalen zijn DRQ0 t/m DRQ7 genoemd.

De DMA-kanalen worden alsvolgt gebruikt.

DRQ0 Geen standaard funktie.
DRQ1 Geen standaard funktie.
DRQ2 Floppy-disk controller.
DRQ3 Geen standaard funktie.

DRQ4 Cascade voor gebruik van tweede DMA-controller.
DRQ5 Geen standaard funktie.
DRQ6 Geen standaard funktie.
DRQ7 Geen standaard funktie.

De DMA-kanalen DRQ1 t/m DRQ3 worden naar de 8 bits slots geleid, overeenkomstig het P3101 en P3102 slot. Een 16 bits slot beschikt over de DMA-kanalen DRQ0 t/m DRQ3 en DRQ5 t/m DRQ7.

3. Overzicht P3101 en P3102.

Type Kaart	I/O-poorten		Interrupt		DMA-kanaal		Geheugen
	Standaard	Alternatief	Standaard	Alternatief	Standaard	Alternatief	
Corona harddisk controller. 1)	300-307	-	-	-	-	-	-
Western Digital controller.	320-323	-	IRQ5	-	DRQ3	-	C8000-C9FFF
Intern serie interface COM1.	3F8-3FF	-	IRQ4	-	-	-	-
Extern serie interface COM2.	2F8-2FF	-	IRQ3	-	-	-	-
Intern parallel int. LPT1.	3BD-3BE	-	(IRQ7)	-	-	-	-
Extern parallel int. LPT2.	378-37A	-	(IRQ7) 3)	(IRQ5) 3)	-	-	-
Extern parallel int. LPT3.	278-27A	-	-	-	-	-	-
Interne flex. disk contr.	3F4-3F5	-	IRQ6	-	DRQ2	-	-
	3F2	-	-	-	-	-	-
Interne monochroom video.	3B4-3B5	-	-	-	-	-	B0000-B0FFF
	3B8-3BA	-	-	-	-	-	-
	3F7 2)	-	-	-	-	-	-
Interne timer.	40-43	-	IRQ0	-	DRQ0	-	-
Toetsenbord.	60-63	-	IRQ1	-	-	-	-
Gereserveerde I/O poorten.	00-EF	-	-	-	-	-	-
Quadram kleurenkaart.	3D0-3DF	-	-	-	-	-	B8000-BFFFF
Persyst kleurenkaart.	3D4-3D5	-	-	-	-	-	B8000-BFFFF
	3D8-3DC	-	-	-	-	-	-
VOTAN-kaart.	280-28F	2C0-2CF	IRQ3	IRQ2	-	-	-
	-	340-34F	-	IRQ4	-	-	-
	-	390-39F	-	-	-	-	-
Synchrone DC-kaart.	380-383	-	IRQ7	-	-	-	-
Powerboard 4 1)							
Klok-kalender funktie.	210-212	310-312	-	-	-	-	-
COM2 Funktie.	2F8-2FF	-	IRQ3	-	-	-	-
Persyst multifunktie kaart.							
Geheugen funktie.	-	-	-	-	-	-	80000-9FFFF
Klok-kalender funktie.	350-35F	-	-	-	-	-	-
COM2 funktie.	2F8-2FF	-	IRQ3	-	-	-	-
LPT2 funktie.	378-37A	-	(IRQ7)	-	-	-	-
CXI-kaart.	3EE-3EF	2EE-2EF	-	-	DRQ1	DRQ3	-
LWSI-contr. (Zonder mod.)	-	-	-	-	-	-	*80000-85FFF
LWSI-contr. (Na modificatie)	-	-	-	-	-	-	D0000-D5FFF
LAN-controller ILP #0 (Mem 1)	364-267	-	IRQ2	IRQ3	-	-	D0000-DFFFF
LAN-controller ILP #0 (Mem 2)	364-267	-	IRQ2	IRQ3	-	-	E0000-EFFFF
Tape-controller Archive	200-203	Diversen	IRQ3	IRQ2	DRQ1	-	-
	-	-	-	IRQ4	-	-	-
	-	-	-	IRQ7	-	-	-

1) Uniek voor P3101.
2) Uniek voor P3102.
3) Hangt af van type LPT2 kaart.
(IRQ.) Interrupt lijn is wel gereserveerd, maar wordt nooit voor deze functie gebruikt.

4. Overzicht P3200.

Type Kaart	I/O-poorten		Interrupt		DMA-kanaal		Geheugen
	Standaard	Alternatief	Standaard	Alternatief	Standaard	Alternatief	
Western Digital controller.							
Harddisk funktie.	1F0-1F7	170-177	IRQ14	-	-	-	-
	3F6	376	-	-	-	-	-
Flex. disk funktie.	3F2	-	IRQ6	-	DRQ2	-	-
	3F4-3F5	-	-	-	-	-	-
Extern serie interface COM1.	3F8-3FF	-	IRQ4	-	-	-	-
Extern serie interface COM2.	2F8-2FF	-	IRQ3	-	-	-	-
Extern parallel int. LPT1.	3BD-3BE	-	(IRQ7)	-	-	-	-
Extern parallel int. LPT2.	378-37A	-	(IRQ5) 1)	(IRQ7) 1)	-	-	-
Extern parallel int. LPT3.	278-27A	-	-	-	-	-	-
Interne timer.	40-43	-	IRQ0	-	-	-	-
Toetsenbord.	60	-	IRQ1	-	-	-	-
Co-processor 80287.	F0-F1	-	IRQ13	-	-	-	-
	F8-FF	-	-	-	-	-	-
Interne Klok-kalender.	70-71	-	IRQ8	-	-	-	-
Gereserveerde I/O poorten.	00-FF	-	-	-	-	-	-
Everex monochroom video kaart.							
Halve configiratie.	3B0-3BF	-	-	-	-	-	B0000-B7FFF
Volle configuratie.	3B0-3BF	-	-	-	-	-	B0000-BFFFF
Persyst kleurenkaart.	3D4-3D5	-	-	-	-	-	B8000-BFFFF
	3D8-3DF	-	-	-	-	-	-
MAD Standaard video kaart.							
Monochroom gebruik.	3B4-3BF	-	-	-	-	-	B0000-B3FFF
Kleuren gebruik.	3D0-3DF	-	-	-	-	-	B8000-BBFFF
VOTAN-kaart.	280-28F	2C0-2CF	IRQ3	IRQ2	-	-	-
	-	340-34F	-	IRQ4	-	-	-
	-	390-39F	-	-	-	-	-
Synchrone DC-kaart.	380-383	-	IRQ7	-	-	-	-
CXI-kaart.	3EE-2EF	2EE-3EF	-	-	DRQ1	DRQ3	-
LWSI-contr. (Zonder mod.)	-	-	-	-	-	-	80000-85FFF
LWSI-contr. (Na modificatie)	-	-	-	-	-	-	D0000-D5FFF
LAN-controller ILP #0	364-267	-	IRQ9	IRQ3	-	-	D0000-DFFFF
Tape-controller Archive	200-203	Diversen	IRQ3	IRQ2 via 9	DRQ1	DRQ3	-
	-	-	-	IRQ4	-	-	-
	-	-	-	IRQ5	-	-	-
	-	-	-	IRQ7	-	-	-

1) Hangt af van type LPT2 kaart.
(IRQ.) Interrupt lijn is wel gereserveerd, maar wordt nooit voor deze functie gebruikt.

Groeten, Peter van Brakel.